1 SYSTEM OVERVIEW

SERIAL 5101 ONWARDS.

The CRAY Y-MP EL computer system is a completely self-contained system. This means that the central processing unit (CPU), input/output subsystem (IOS), and all peripherals can be contained in one cabinet. The cabinet can be installed easily in most general office environments equipped with a 200- to 250-Vac power source. (47-63 Hz) 30 Amp/phase.

One to four CPU boards can be installed in the CRAY Y-MP EL primary cabinet. This cabinet also holds four memory boards, an IOS constructed from a Versabus Modular Eurocard (VMEbus)-based assembly, and the optional peripherals as requested by the customer. Another component in the primary cabinet is the small computer system interface (SCSI) subsystem. The SCSI subsystem consists of a cartridge-type streaming tape drive, a 780-Mbyte hard disk drive, and an 8-mm helical scan tape drive. The SCSI tape drives are used to install any new releases of software as they become available. It can also perform data transfers and is the system backup and boot device.

The primary cabinet is designed so that another standard cabinet can be bolted to the primary cabinet to expand the system. It is possible to connect as many as three expansion cabinets to the primary cabinet, allowing for IOS and peripheral expansion.

Figure 1-1 shows how three expansion cabinets are configured with the CRAY Y-MP EL system. Figure 1-2 shows a two-cabinet CRAY Y-MP EL system.

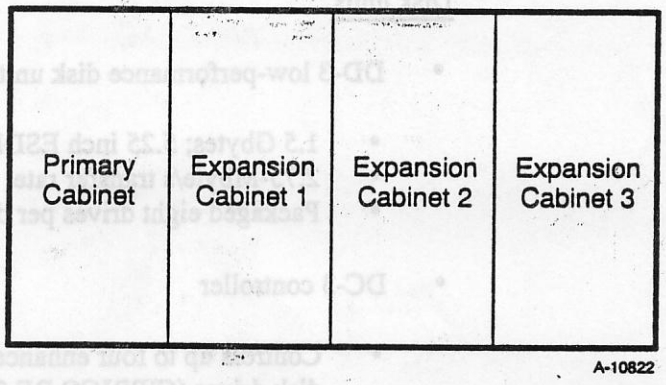


Figure 1-1. Left Side View (Maximum Configuration)

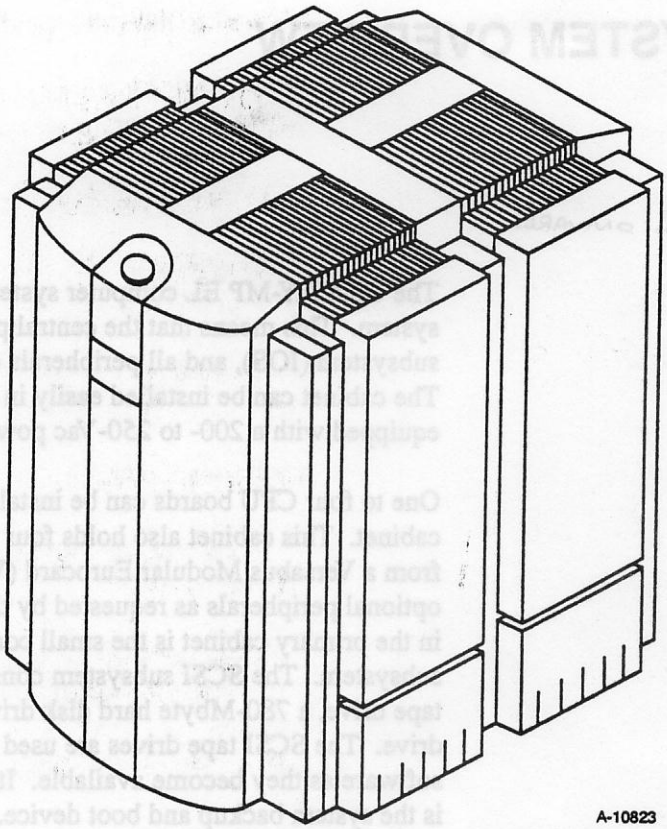


Figure 1-2. CRAY Y-MP EL Computer System

All of the cabinets forming the CRAY Y-MP EL system are air cooled by integrated fans at both the top and bottom of the frame. This form of cooling is referred to as vertical cooling.

The peripheral devices available on the CRAY Y-MP EL system and their characteristics are listed below.

Disk units

- DD-3 low-performance disk unit
  - 1.5 Gbytes; 5.25 inch ESDI drive
  - 2.75-Mbyte/s transfer rate
  - Packaged eight drives per drawer with a shared power supply
- DC-3 controller
  - Controls up to four enhanced serial drive interface (ESDI) disk drives (CIPRICO RF-3411)
  - Each disk controller provides error correction code (ECC) and media defect management

- DD-4 medium-performance disk unit
  - 3.0 Gbyte 8-inch two-head intelligent peripheral interface (IPI) dual port disk drive
  - 9.34 Mbytes/s transfer rate
  - Packaged two disk drives per drawer with one power supply per drive
  - DC-4 controller controls IPI-2 containing two IPI channels; each channel can handle two DD-4 disk drives
- DAS-2 disk array subsystem
  - Intelligent disk array controller (bus master by Maximum Strategy, Inc.)
  - Bank of eight 1.5-Gbyte ESDIs for storage, plus one for parity and one spare
  - Hardware striping used to distribute data evenly across all drives
  - Sustained transfer rate of 13 Mbytes/s
  - Has 12-Gbyte unformatted capacity

Tape units

- 9-track tape drive subsystem
  - One TCU-2 tape controller unit (CIPRICO TM-3000)
  - One TD-2 800 bpi (NRZI), 1600 bpi (PE), 6250 bpi (GCR) 9-track low profile tape drive, 125 ips
- Cartridge tape drive (EXABYTE) models RST 1
  - EX-1 2.3 Gbyte, EXB-8200 246K/s 8-mm tape drive
  - EX-2 5.0 Gbyte, EXB-8500 500K/s 8-mm tape drive
- TD-3 0.5-inch cartridge tape drive; 3480-compatible tape
  - One SCSI peripheral controller (SI-1)
  - One 18-track tape drive in low-profile configuration

- DR-1 removable disk system
  - Dual 5.25-inch disks in easily removable cartridges designed to protect data from damage during transport
- DR-2 removable IOS disk drive

Customers select peripheral devices according to their requirements.

CPU Overview

The CPU in the CRAY Y-MP EL computer system is located on a single 16 x 22 inch printed circuit (PC) board. This PC board contains all of the logic associated with the CRAY Y-MP EL system CPU. Very large scale integration (VLSI) solid-state technology enables a relatively small PC board to contain an entire CPU.

The VLSI chips used in the CPU are application-specific integrated circuits (ASICs). They are constructed using complementary metal oxide semiconductors (CMOS). The ASICs are available in a single package size with 299 pins. The internal construction of the ASIC consists of 100,000 undefined gates. This massive number of gates is contained in a 2 x 2 inch package, which consumes an average of 5 watts at + 5 volts.

The CPU contains 23 separate ASICs consisting of nine application types. Figure 1-3 shows the chip layout for the CPU board of the CRAY Y-MP EL system.

The nine types of ASICs that form the CPU are:

- 1 arbiter ASIC (AR), used for memory access control and for inter-CPU synchronization.
- 1 address and scalar ASIC (AS), containing the address registers, address functional units, scalar registers, and scalar functional units.
- 2 channel control ASICs (CCs). Each CC supports two Y1 channels, which are the 40-Mbyte/s channels that connect to the VMEbus subsystem. The CC is also used for control support.
- 8 data switch ASICs (DSs), which perform the major data steering between memory, channel, and functional units; they contain the vector registers and B/T registers.

- 4 execution unit ASICs (EUs). Each EU contains all of the vector and floating-point functional units, except the floating-point reciprocal. All of these functional units are fully pipelined, but only one functional unit can be active per EU at any one time. Vector mask (VM) operations can only be performed on EU3.

- 1 memory control ASIC (MC), which provides memory address generation for a maximum of 512 Mwords of memory. The MC also performs operand and program range error detection.

- 4 memory data ASICs (MDs), which perform single-error correction/double-error detection (SECDED †) and generate check bits. The MDs also support any memory maintenance instructions.

- 1 processor control ASIC (PC). This device contains eight 32-word instruction buffers (IBs), performs shared register (SR) access control, and supports 7 shared register clusters. Also included are the instruction issue control circuits, including the instruction and functional unit scoreboard, and I/O interrupt handling circuits.

- 1 reciprocal and console ASIC (RC). The RC performs floating-point reciprocal approximations and contains console bus interfaces, scan control and clock control hardware, and console registers.

The interconnection of these CPU components is shown in Figure 1-4.

The CRAY Y-MP EL system is designed to contain up to four independent CPUs. However, the four CPUs can work in conjunction by using shared registers or using the common memory section. The CPU runs on a 30-nanosecond (ns) clock. Each CPU connects to the system backplane using 1230 signal pins.

† Hamming, R. W. "Error Detection and Correcting Codes." *Bell System Technical Journal.* 29.2 (1950): 147-160.

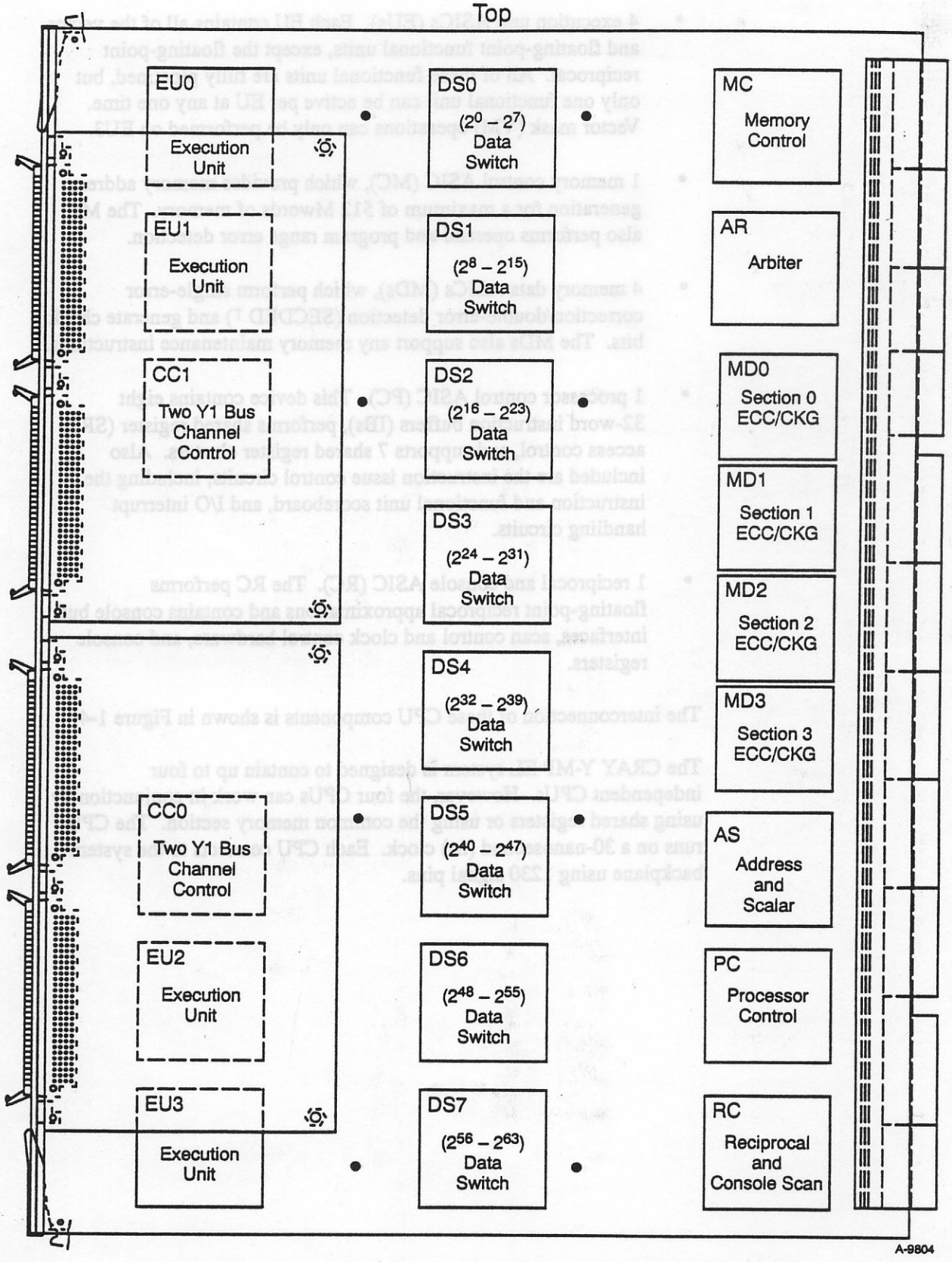
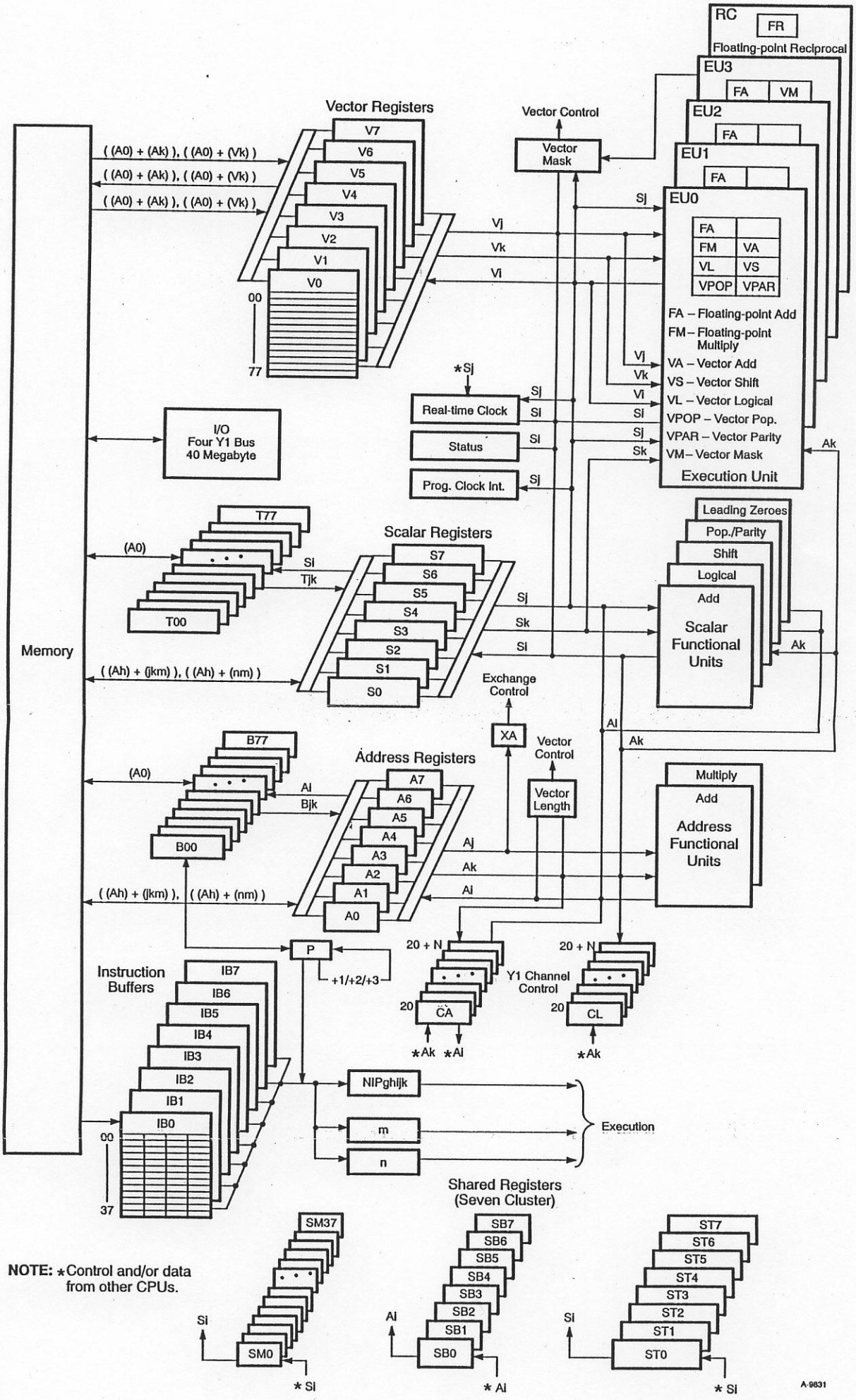


Figure 1-3. CPU/Channel Module



NOTE: *Control and/or data from other CPUs.

Figure 1-4. CRAY Y-MP EL Block Diagram

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Memory Overview

Central memory in the CRAY Y-MP EL system is contained on four PC boards. Each of these boards is 16 x 22 inches (the same size as the CPU board) and is composed of two ASIC types used for data control and fanout, with a total of nine ASICs per board and a specific number of 1M x 4 dynamic random access memory integrated circuits (DRAMs). The number of DRAMs depends upon the customer's choice of available memory options.

The CRAY Y-MP EL system can be ordered with a 32-Mword, a 64-Mword, or a 128-Mword central memory. In the case of the 32-Mword or 64-Mword options, the memory PC boards are half-populated modules. The difference between the 32-Mword and the 64-Mword memory options is that on the 32-Mword board, an address line is eliminated, effectively reducing the chip capacity. When the 32-Mword option is selected, a memory module contains 8 Mwords of memory supplied by 288 DRAMs. The 64 Mword memory option also contains 288 DRAMs, but provides 16 Mwords of memory per module. The third option, 128 Mword memory, is formed with 576 DRAMs per memory module, creating 32 Mwords per module. This 128-Mword option uses the full capacity of the memory module, and is considered to be fully populated.

The CRAY Y-MP EL system central memory contains a total of 64 banks spread across the four modules. Each module contains 16 banks and is considered a memory section. These 16 banks are separated into lower and upper banks on each board. Thus, a half-populated memory board uses only the lower bank, but still retains the full 16 banks of memory. This means that a fully populated memory module uses both upper and lower banks.

The layout of the memory board is shown in Figure 1-5. The two ASIC types used on the memory board are:

- 2 memory array control ASICs (MACs) support the four memory functions. These ASICs contain an address crossbar that allows access to memory from each of the four CPUs as well as refresh address counters for the local refresh function. The MACs also contain DRAM address and control circuitry, which provides control to all memory array data ASICs.

- 7 memory array data ASICs (MADs). These ASICs contain a data crossbar that connects the four CPUs to the 16 banks contained on each memory board. The MADs handle a portion of the 72-bit memory data word.

Figure 1-6 shows the chassis locations of the eight boards that form the CRAY Y-MP EL computer system. Note that this represents a top view, with the front of the chassis at the bottom of the diagram.

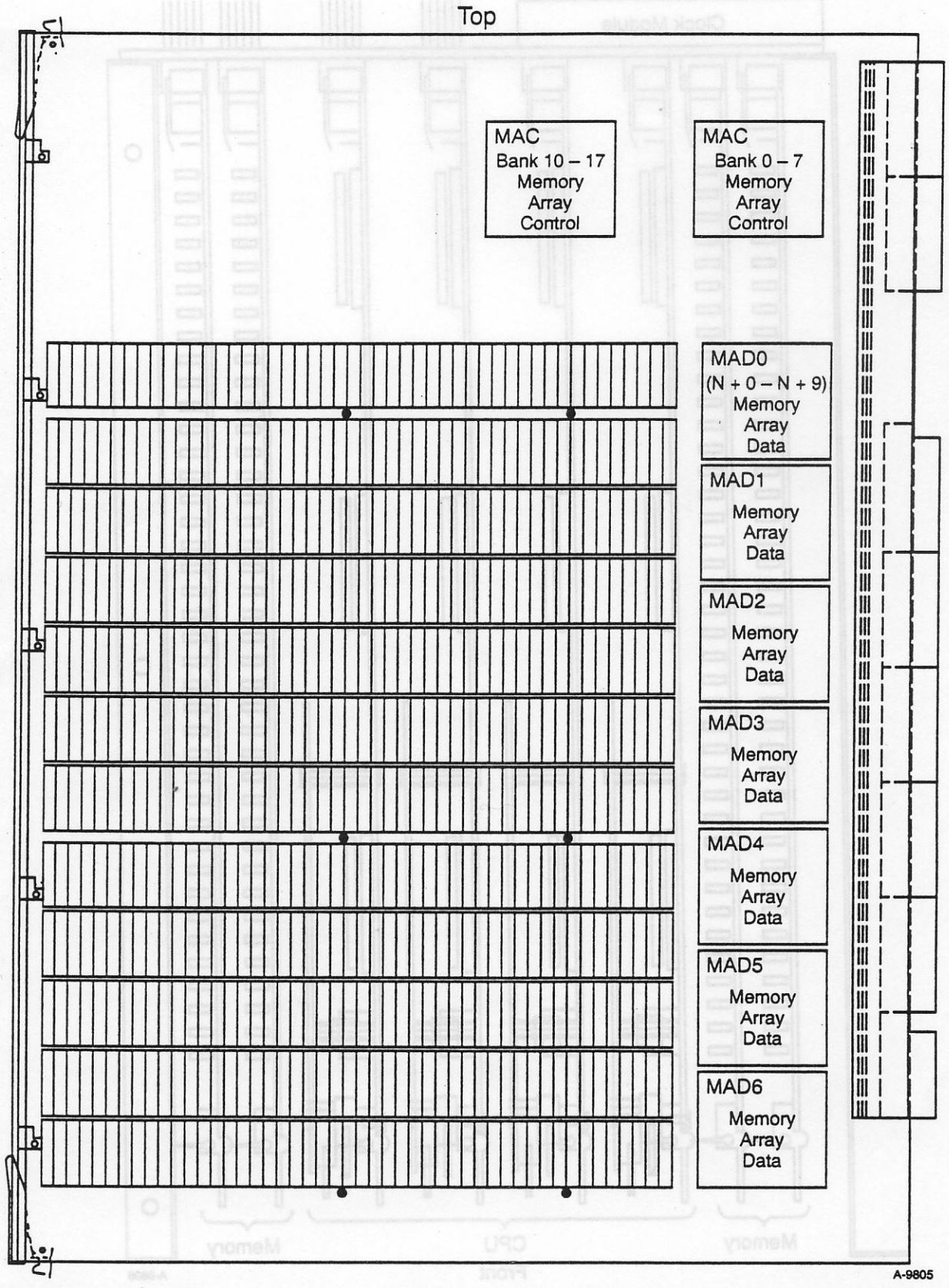

Figure 1-5. Memory Module

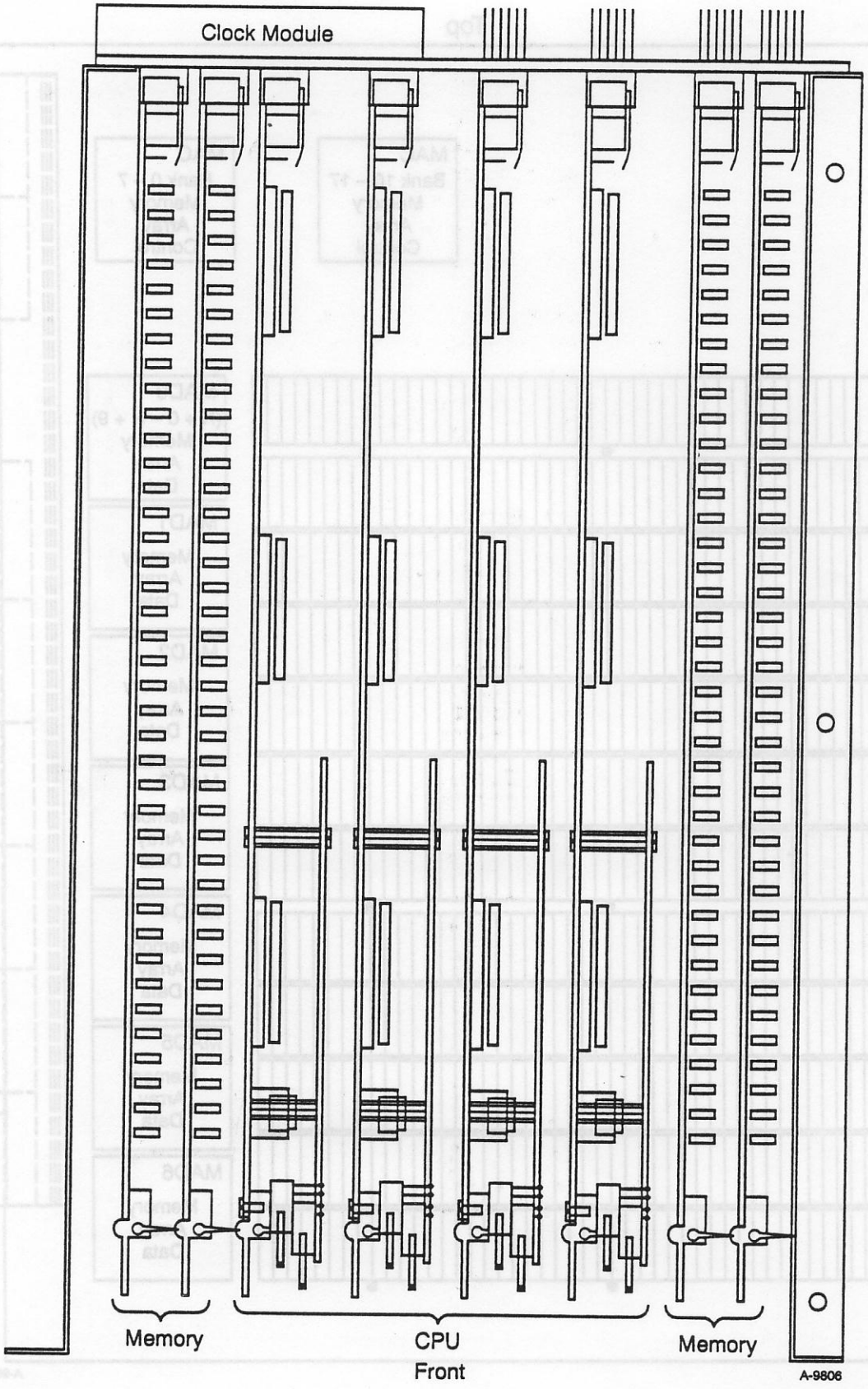

Figure 1-6. Chassis, Top View

Input/Output Subsystem Overview

The IOS for the CRAY Y-MP EL system was selected to provide customers with the maximum choice of peripheral equipment. The IOS is a VME-based system that communicates with the CPU via the Y1 bus (a 40-Mbyte/s channel) connected to the input/output buffer board (IOBB). The IOBB is the only Cray Research, Inc. proprietary board within the IOS. All other functions within the IOS are performed using vendor-supplied VME boards.

The restrictions of the IOS configuration require use of a 68030-type processor that is capable of processing 32 bits, and as many as eight peripheral controllers to handle data transfers. A possible IOS configuration is represented in Figure 1-7. The types of controllers used are defined by the customer's choice of system peripherals.

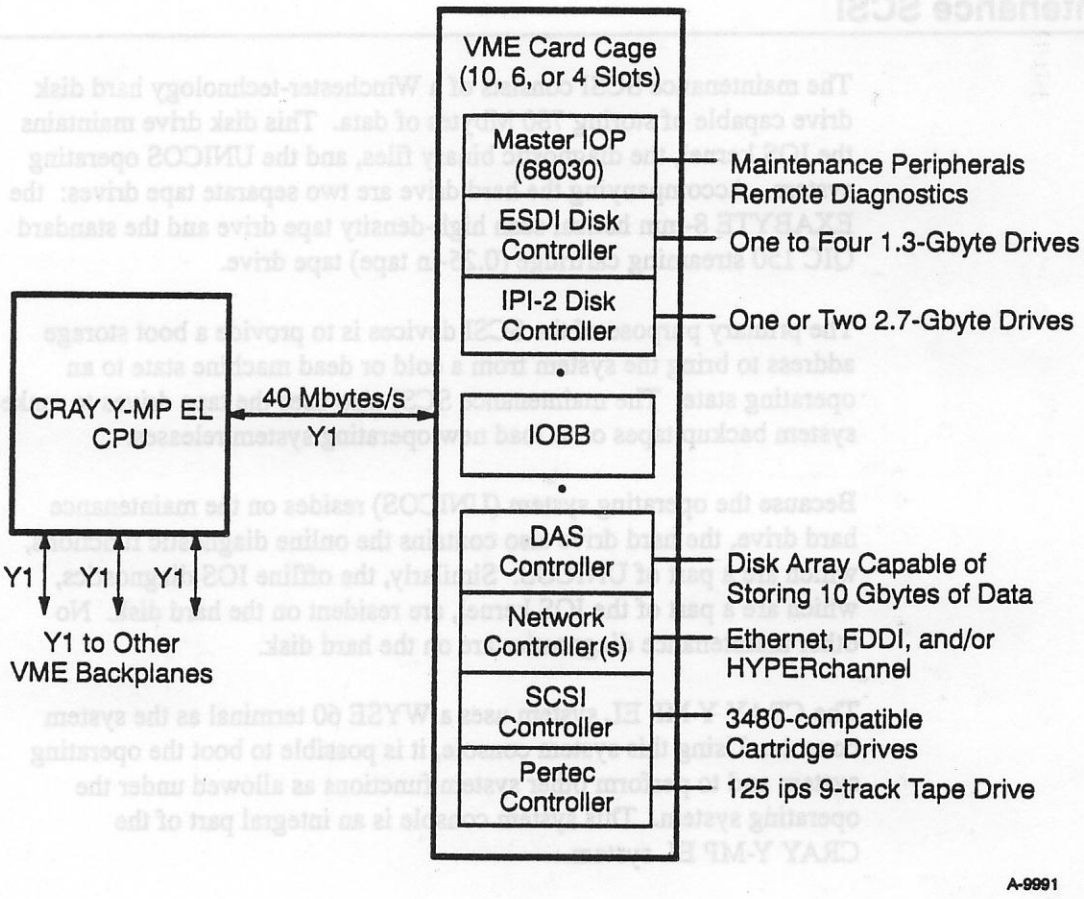

Figure 1-7. IOS Configuration

The standard VME mechanical chassis is a 19-inch rack mount chassis that is air cooled, supports standard 6U x 160 mm VME boards, and requires a 750-watt power supply. The backplane is a modular design based on a 10-slot system. The backplane configurations include:

- 10 slots + 10 slots option
- 10 slots + 6 slots + 4 slots option
- 6 slots + 4 slots + 6 slots + 4 slots option

Each cabinet within the CRAY Y-MP EL system contains a VMEbus chassis. In its maximum configuration, this VMEbus can be separated into the 6-slot, 4-slot, 6-slot, 4-slot option, resulting in a maximum of 16 IOS configurations (4 cabinets x 4 IOSs per cabinet = 16 IOSs per system). The customer decides how many IOSs to include in a system, depending on desired performance.

The Maintenance SCSI

The maintenance SCSI consists of a Winchester-technology hard disk drive capable of storing 780 Mbytes of data. This disk drive maintains the IOS kernel, the diagnostic binary files, and the UNICOS operating system. Accompanying the hard drive are two separate tape drives: the EXABYTE 8-mm helical scan high-density tape drive and the standard QIC 150 streaming cartridge (0.25-in tape) tape drive.

The primary purpose of the SCSI devices is to provide a boot storage address to bring the system from a cold or dead machine state to an operating state. The maintenance SCSI also uses the tape drives to make system backup tapes or to load new operating system releases.

Because the operating system (UNICOS) resides on the maintenance hard drive, the hard drive also contains the online diagnostic functions, which are a part of UNICOS. Similarly, the offline IOS diagnostics, which are a part of the IOS kernel, are resident on the hard disk. No other maintenance diagnostics are on the hard disk.

The CRAY Y-MP EL system uses a WYSE 60 terminal as the system console. Using this system console, it is possible to boot the operating system and to perform other system functions as allowed under the operating system. This system console is an integral part of the CRAY Y-MP EL system.

The proprietary maintenance workstation, or the MWS-EL, is connected to a separate input bus. This workstation is a Sun 4/40, and is not considered part of the CRAY Y-MP EL system. Instead, the MWS-EL is owned by the maintenance organization and is available for maintenance representative use only. This workstation provides a remote access

connection from the maintenance hub, and in the case of an on-site visit from a maintenance representative, provides a platform for maintenance functions.

The MWS-EL contains a hard disk drive with a complete copy of the mainframe maintenance environment (MME), which is used to isolate problems in the CPU or memory using the offline diagnostics available to the CRAY Y-MP EL system.

The MWS-EL is connected to the CRAY Y-MP EL system via an RS-422 connection that connects to the Heurikon V68/K30 IOS controller board in each of the incorporated IOSs. The Heurikon board, used as the IOS master processor in the IOS 0 location, acts as the MWS-EL arbitrator, and is required in that location for correct MWS-EL operation. However, all IOSs are accessible to the MWS-EL individually.

2 CENTRAL PROCESSING UNIT

30 nanosecond clock

The CRAY Y-MP EL computer system central processing unit (CPU) is a single printed circuit (PC) board module that contains all the registers and functional units normally used in a computer mainframe. This miniaturization is made possible by very large-scale integration (VLSI) complimentary metal oxide semiconductive (CMOS) application-specific integrated circuits (ASICs). Twenty-three of these ASICs are mounted on a single 16 x 22 x .093 inch PC board.

The CMOS ASICs are 1-micron, two-layer devices with 100,000 undefined gates and 299 pins, each measuring 2.08 x 2.08 inches. The power consumed by these chips averages less than 5 watts per ASIC, operating at + 5 volts.

The PC board used to form the CPU module is manufactured of 16 separate layers:

- 1 top pad
- 1 bottom pad
- 4 ground (Vss) layers
- 4 power (Vdd) layers
- 6 signal layers

This module uses an average of 160 watts of power per CPU module. Therefore, the maximum of four CPU modules in a system consumes 640 watts. The CPU, like the entire CRAY Y-MP EL system, is an air cooled device.

The following nine types of ASIC chips reside on the CPU module:

- One arbiter ASIC (AR) controls memory access and arbitrates all memory conflicts. It also provides interrupting CPU synchronization.

- One address and scalar ASIC (AS) contains all of the address registers and the address functional units (FUs), as well as the scalar (S) registers and scalar FUs.

- Two channel control ASICs (CC) control or support the functions of two Y1 channels. Each of the Y1 channels is capable of 40-Mbyte/s transfers and each connects to a VME subsystem. It is also possible to use two Y1 channels in conjunction to provide one high-performance parallel interface (HIPPI) channel for 100-Mbyte/s transfers). The CC chip also contains the console bus interface, which provides console support. This function is only implemented on CC0.

- Eight data switch ASICs (DS) steer data between memory, the selected channel, and the required FUs. The DSs also contain the vector registers and some selected exchange registers.

- Four execution unit ASICs (EU) contain all of the vector and floating-point FUs, with the exception of the floating-point reciprocal FU. This format provides full pipelining to the EU chips and allows each to work on a different problem independently of the others.

  The EU pipeline varies from a standard pipeline. When the EU is used as a series pipeline, the results of the computational operation must be returned to the DS ASIC, where the result data is steered before it can be used as an operand in a continuing computation.

  When the EUs are used in parallel pipelines, it is possible to use all four simultaneously. In this instance, the results of the individual computations can be used in a chaining operation as continuation operands. The restrictions that pertain to the EU chips are:

  - Only one FU in each EU chip can be operating at any one time
  - Only the EU3 ASIC is capable of executing vector mask (VM) instructions (146 and 147, 175 instructions)

- One memory control ASIC (MC) provides address generation, which can support up to 512 Mwords of memory. The MC chip also provides both operand and program range error detection.

- Four memory data ASICs (MD) perform single-error correction, double-error detection (SECDED) functions, including check bit generation on the read and write memory data. The MDs are also used to support all of the memory maintenance instructions.

- One processor control ASIC (PC) contains the CPU instruction buffers. The CRAY Y-MP EL system CPU uses eight instruction buffers, each of which is 32 words wide. Instruction issue control and I/O interrupt handling control also reside on the PC chip. Part of the issue control function is a resource scoreboard, which also resides on the PC. Shared register access control is also performed on the PC ASIC (the CRAY Y-MP EL system supports seven shared register clusters).

- One reciprocal and control ASIC (RC) contains the floating-point reciprocal FU, the scan and clock control, and the control registers.

These units interconnect in the way shown on the CRAY Y-MP EL system block diagram, Figure 2-1. The signal paths are shown in more detail in Figure 2-2, a block diagram of the CPU bus. This diagram also shows the internal contents of each of the ASICs located on the CPU module. Figure 2-3 shows the actual location of the various ASICs on the CPU module.

The CRAY Y-MP EL system supports one to four CPUs. Each of these CPUs can support up to four VME subsystems. The CPU module is completely self contained and plugs into the mainframe backplane using 11 connectors that provide 1230 signal pins.

When a CPU is indicated as the faulty unit in an incident, the only onsite repair performed is the replacement of the CPU module.

The CPU module connects to the mainframe memory via four 72-bit bidirectional ports. Each of these ports connects to a separate memory section. Each of the CPU modules in a CRAY Y-MP EL system contains a copy of all memory and shared register reservations, to reduce the possibility of conflicts. Each CPU has to check its local request registers, not the request registers of all of the CPUs.

Support for multiple CPUs in the mainframe includes:

- Shared memory
- Shared registers
- Shared I/O channels
- Deadlock detection
- Shared deadstart paths

However, the CRAY Y-MP EL system does not currently support:

- Performance monitors
- High-speed (HISP) channels
- Very high-speed (VHISP) channels

Some instructions are discussed in this section, with several specific examples. Refer to Appendix A for a list of the instructions that are valid for the CRAY Y-MP EL system.

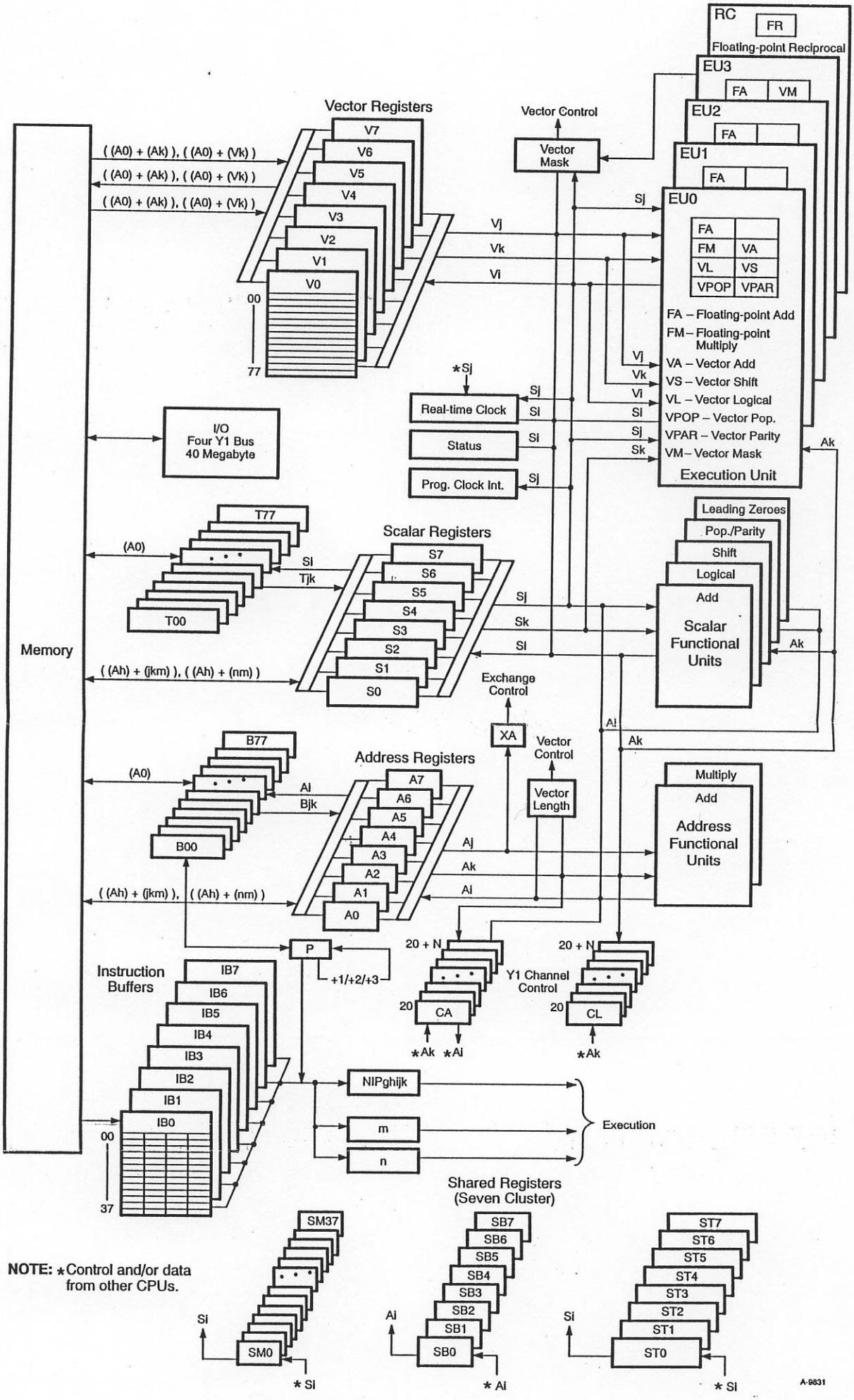

Figure 2-1. CRAY Y-MP EL Block Diagram

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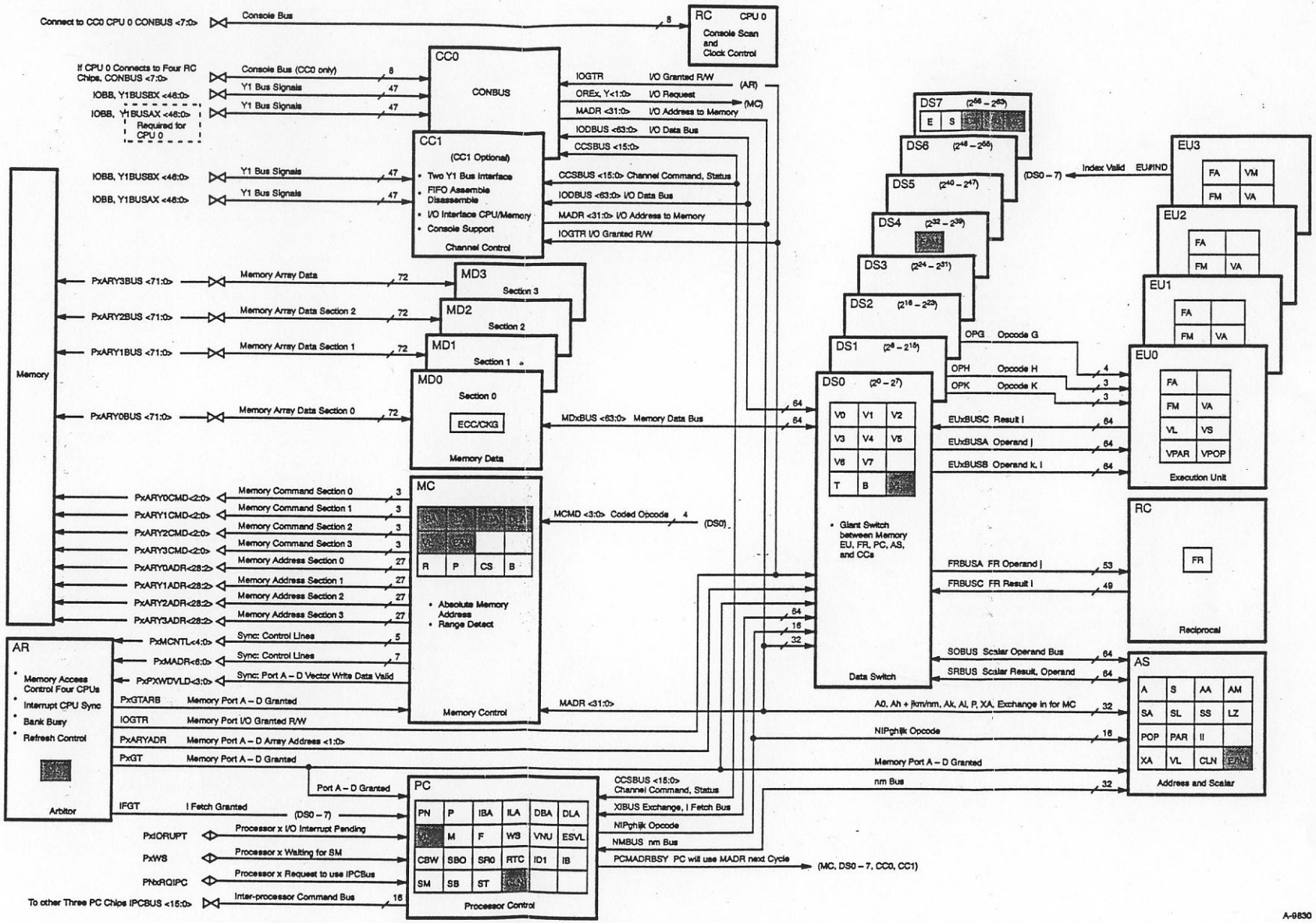

Figure 2-2. CPU Bus Block Diagram

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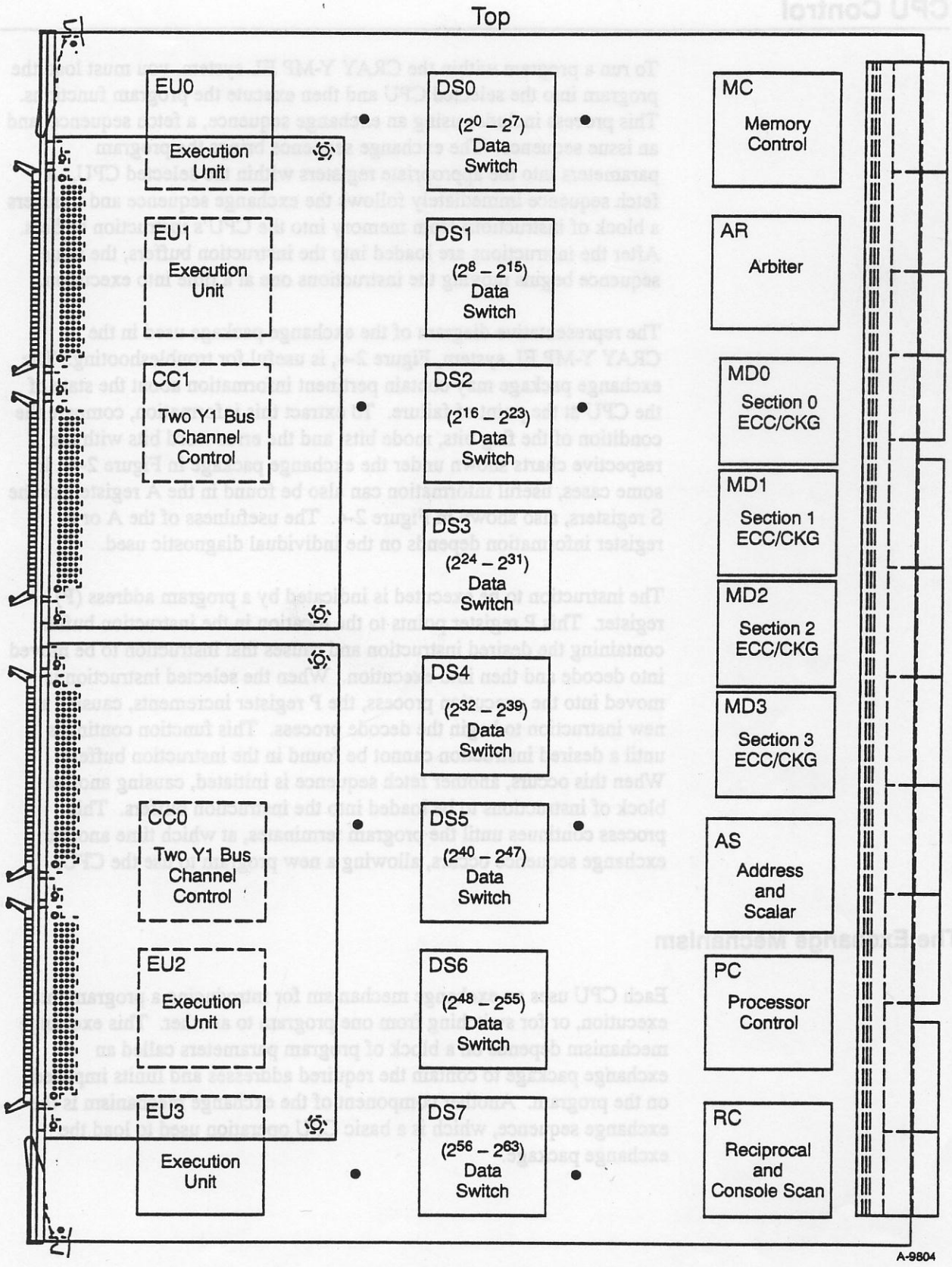


Figure 2-3. CPU Module

CPU Control

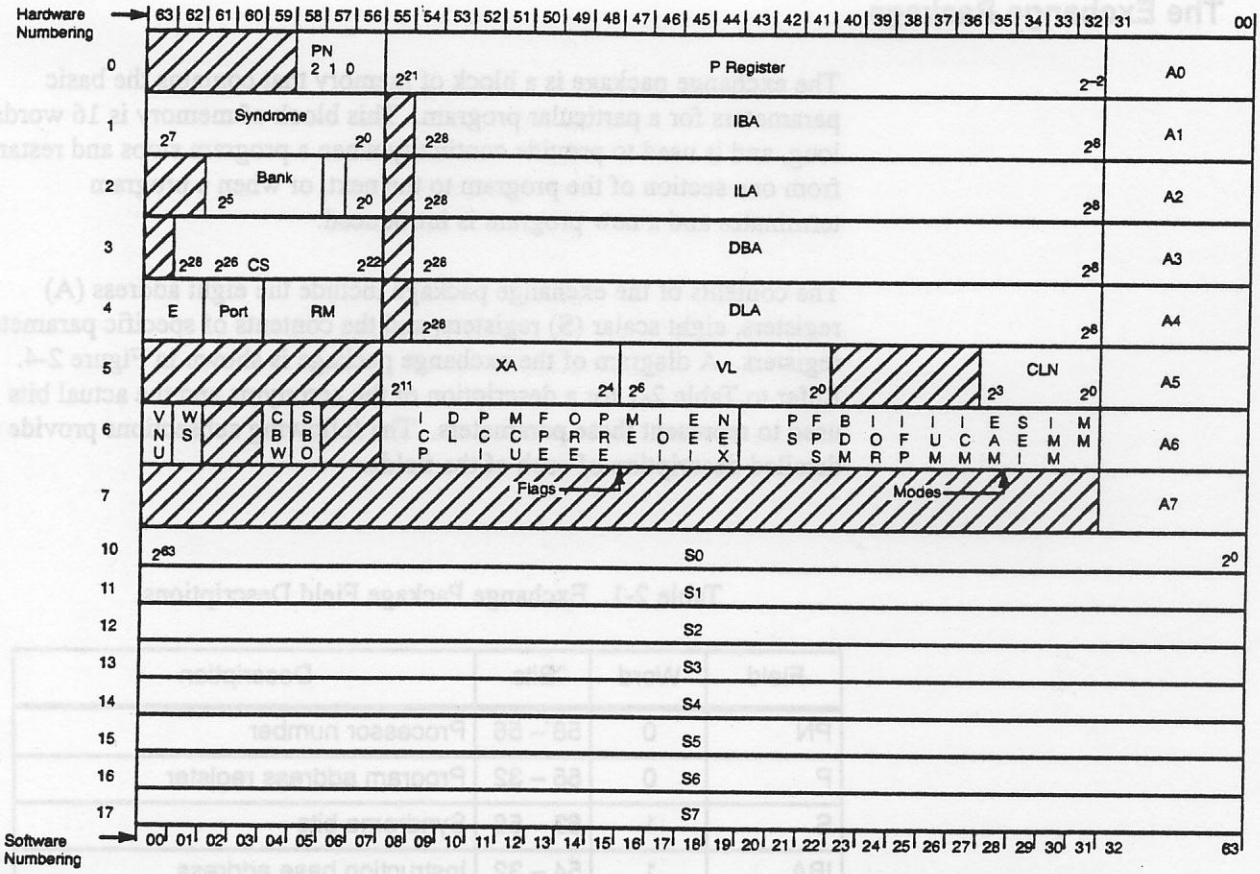
To run a program within the CRAY Y-MP EL system, you must load the program into the selected CPU and then execute the program functions. This process includes using an exchange sequence, a fetch sequence, and an issue sequence. The exchange sequence brings the program parameters into the appropriate registers within the selected CPU. A fetch sequence immediately follows the exchange sequence and transfers a block of instructions from memory into the CPU's instruction buffers. After the instructions are loaded into the instruction buffers, the issue sequence begins moving the instructions one at a time into execution.

The representative diagram of the exchange package used in the CRAY Y-MP EL system, Figure 2-4, is useful for troubleshooting. The exchange package may contain pertinent information about the state of the CPU at the point of failure. To extract this information, compare the condition of the flag bits, mode bits, and the error word bits with the respective charts shown under the exchange package in Figure 2-4. In some cases, useful information can also be found in the A registers or the S registers, also shown in Figure 2-4. The usefulness of the A or S register information depends on the individual diagnostic used.

The instruction to be executed is indicated by a program address (P) register. This P register points to the location in the instruction buffer containing the desired instruction and causes that instruction to be moved into decode and then into execution. When the selected instruction is moved into the execution process, the P register increments, causing a new instruction to begin the decode process. This function continues until a desired instruction cannot be found in the instruction buffers. When this occurs, another fetch sequence is initiated, causing another block of instructions to be loaded into the instruction buffers. This process continues until the program terminates, at which time another exchange sequence occurs, allowing a new program to use the CPU.

The Exchange Mechanism

Each CPU uses an exchange mechanism for introducing a program into execution, or for switching from one program to another. This exchange mechanism depends on a block of program parameters called an exchange package to contain the required addresses and limits imposed on the program. Another component of the exchange mechanism is the exchange sequence, which is a basic CPU operation used to load the exchange package.



Word 6		Flag Bits	Cause Exchange
55		Reserved	
54	ICP	Interrupt from Internal CPU	MM'
53	DL	Deadlock Interrupt	MM' and IMM
52	PCI	Programmable Clock Interrupt (staged)	MM'
51	MCU	MCU Interrupt	MM'
50	FPE	Floating-point Error Interrupt	MM and IMM
49	ORE	Operand Range Error Interrupt	MM' and IMM
48	PRE	Program Range Error Interrupt	MM' and IMM
47	ME	Memory Error Interrupt	Always
46	IOI	I/O Interrupt (staged)	MM'
45	EEI	Error Exit Interrupt	Always
44	NEX	Normal Exit Interrupt	Always

Word 6		Mode Bits
63	VNU	Vectors Not Used
62	WS	Waiting on Semaphores
59	CBW	Concurrent Block Write (CRAY Y-MP EL System only)
58	SBO	Scalar and Block Overlap (CRAY Y-MP EL System only)
43		Reserved
42	PS	Program State
41	FPS	Floating-point Status
40	BDM	Bidirectional Memory
39	IOR	Interrupt Operand Range Error
38	IFP	Interrupt Floating-point Error
37	IUM	Interrupt Uncorrectable Memory
36	ICM	Interrupt Correctable Memory
35	EAM	Extended Address Mode (32-bit)
34	SEI	Selected External Interrupt
33	IMM	Interrupt Monitor Mode
32	MM	Monitor Mode

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Figure 2-4. Exchange Package

The Exchange Package

The exchange package is a block of memory that contains the basic parameters for a particular program. This block of memory is 16 words long, and is used to provide continuity when a program stops and restarts from one section of the program to the next, or when a program terminates and a new program is introduced.

The contents of the exchange package include the eight address (A) registers, eight scalar (S) registers, and the contents of specific parameter registers. A diagram of the exchange package is shown in Figure 2-4. Refer to Table 2-1 for a description of the acronyms and the actual bits used to represent these parameters. The following subsections provide a detailed description of each of the fields.

Table 2-1. Exchange Package Field Descriptions

Field	Word	Bits	Description
PN	0	58 – 56	Processor number
P	0	55 – 32	Program address register
S	1	63 – 56	Syndrome bits
IBA	1	54 – 32	Instruction base address
BANK	2	61 – 56	Read address bank
ILA	2	54 – 32	Instruction limit address
CS	3	62 – 56	Read address chip select (bit mask)
DBA	3	54 – 32	Data base address
E	4	63 – 62	Read error type
PORT	4	61 – 60	Port used
RM	4	59 – 56	Read mode
DLA	4	54 – 32	Data limit address
XA	5	55 – 48	Exchange address register
VL	5	47 – 41	Vector length register
CLN	5	35 – 32	Cluster number
VNU	6	63	Vector not used
WS	6	62	Waiting for semaphore
CBW	6	59	Concurrent block write
SBO	6	58	Scalar block overlap

Table 2-1. Exchange Package Field Descriptions (continued)

Field	Word	Bits	Description
FLAGS	6	55 – 44	Flag register
MODES	6	43 – 32	Mode register
A	0 – 7	31 – 0	Address registers
S	10 – 17	63 – 0	Scalar registers

Processor Number Field

The processor number (PN) field indicates which CPU performed the exchange sequence. The value in the PN field is inserted into the exchange package from the backplane. Logical slot 0 contains CPU 0 in the mainframe, logical slot 1 contains CPU 1, etc. Refer to Figure 3-3 for CPU slot configuration.

Program Address Register Field

The program address (P) register contents are stored in the P field of the exchange package. The instruction located at this memory address is the first instruction issued when the program enters the execution phase.

Syndrome Field

The 8-bit syndrome field specifies the syndrome code generated from the SECDED circuits if an error occurs on a memory read operation.

Read Address Bank Field

If an error is detected during a memory read operation, the bank number of the error is retained in the 6-bit read address bank field.

Read Address Chip Select Field

The read address chip select (CS) field identifies the chip in which a memory read error occurs. The CS bit is bit 2^{26} of the memory read address when 1M x 4 DRAM memory chips are used.

Read Error Type Field

The 2-bit read error (E) type field is used to determine the type of memory or I/O error detected. Bit 2^{63} is set if the error is uncorrectable, and bit 2^{62} is set if the error is correctable.

Port Field

The 4-bit port field defines the port where a memory read error or an I/O error occurs. These bits are used with the read mode bits to identify which operation was in progress when the error took place. Refer to Table 2-2 for a translation of these bits.

Table 2-2. Port and Read Mode Field Translation

P Port								RM Read Mode				Port Usage
61	60	61	60	61	60	61	60	59	58	57	56	
A		B		C		D						Exchange
0	0	0	1	1	0	1	1	0	0	0	1	
0	0	0	1	1	0	–	–	0	0	1	0	A or S
–	–	–	–	–	–	D x	x	0	1	0	1	I/O single
–	–	–	–	–	–	D x	x	0	1	1	1	I/O block
0	0	0	1	1	0	–	–	1	0	0	0	B or T
–	–	–	–	–	–	D x	x	1	0	1	1	Fetch
0	0	0	1	1	0	–	–	1	1	0	0	Vector stride
0	0	0	1	1	0	–	–	1	1	1	0	Vector gather/scatter

Read Mode Field

The read mode (RM) field bits are used with the port field bits to determine the read operation that was in progress when a read error occurred. Refer to Table 2-2 for a translation of these bits.

The fields described previously (syndrome, bank, CS, E, port, and RM) are referred to as the memory error data fields. These fields are valid only in the exchange package if one of two conditions are met. The first condition is that the interrupt on correctable memory (ICM) bit must be set in the mode register and a correctable memory error must be detected. This condition causes an exchange to occur. The second condition that

validates the memory error data fields is the interrupt on uncorrectable memory (IUM). This bit must be set in the mode register and an uncorrectable memory error must be detected, causing an exchange to take place. In these two instances, the exchange package contains valid data that can be useful in the repair of the CRAY Y-MP EL system, both at the field replaceable unit (FRU) level and at the component level. When possible, the contents of the exchange package memory error data fields should accompany a memory module when it is returned to central repair for evaluation and component replacement. This information can be in the form of a screen snap when a printer is available, or handwritten when no printer is available.

Data Base Address Register Field

The data base address (DBA) register field is used to hold the base, or first address of the user's data area. The base address is used to determine the location in memory of a program's data. Each time an instruction from the program makes a memory reference, the memory address generated by the instruction is added to the DBA to create the absolute memory address.

On the CRAY Y-MP EL system, the DBA is bit 2^{54} through bit 2^{32}, with bit 2^{32} through bit 2^{39} equal to zero. This condition causes the contents of this register to always be a multiple of 400_8.

Data Limit Address Register Field

The data limit address (DLA) register field holds the highest address of the user's data area and is used to determine the highest absolute memory address a program can use for data. Each time an instruction makes a memory reference, the absolute memory address that is generated is compared to the address held in the DLA. If the absolute memory address is equal to or greater than the DLA value, an out-of-range condition occurs. If the absolute memory address is less than the DLA, the program is allowed to proceed.

If the out-of-range condition occurs during a memory read reference, the reference is allowed to issue and complete, but a zero value is transferred from memory. A memory write reference that exceeds the DLA is allowed to issue, but no memory write occurs.

Instruction Base Address Register Field

The instruction base address (IBA) register field holds the user's base address. This base address is used to determine where a program's instruction area is located in memory. When an instruction fetch

sequence occurs, an absolute memory address is created by adding the relative address generated by the fetch control logic (the upper 22 bits of the P register) to the contents of the IBA register.

Instruction Limit Address Register Field

The instruction limit address (ILA) register field holds the limit address that has been defined as the user's instruction area. The ILA is used to determine the maximum absolute memory address that can be accessed during an instruction fetch sequence.

If the absolute memory address does not fall between the addresses contained in the IBA and the ILA, the CPU generates a program range error interrupt.

Exchange Address Register Field

The exchange address (XA) register field specifies the address of the first word of a 16-word exchange package. The XA register contains the upper 8 bits of a 12-bit area that is used to specify the absolute memory address. The lower 4 bits of this area are forced to zero, causing the conditional requirement for the exchange package to always start on a 16-word boundary. Likewise, the 12-bit limit restricts the exchange package to the lower 10000_8 words of memory.

Vector Length Register Field

The vector length (VL) register field is 7 bits wide and is used to define the length of all vector operations. The length of a vector operation indicates the number of vector elements that are allowed to be used by a vector instruction. The value in the VL register can be changed during program execution by using the 00200*k* instruction. When the VL register is set to zero, the actual number of vector elements used is 100_8 because the VL register is a circular countdown register.

Cluster Number Register Field

The cluster number (CLN) register field is used to determine which cluster of shared registers is used by the CPU executing the program. There are seven clusters of shared registers available for use. These clusters are composed of shared B (SB) registers, shared T (ST) registers, and semaphore (SM) registers. The exchange package contains a number between one and seven in the CLN register field, which determines which cluster of shared registers that CPU can access. To prevent a CPU from accessing any shared registers, a zero is inserted into the CLN field.

Vector Not Used Field

The vector not used (VNU) field reflects the condition of use of the vector instructions 077*ijk* and 140*ijk* through 170*ijk*. If none of these instructions are set in the previous execution interval (that time when the the exchange package was active), then the VNU bit is set. Any time one of the vector instructions is used during the execution interval, VNU is equal to zero.

Waiting for Semaphore Field

When the waiting on semaphore bit is set in the exchange package, it indicates that an exchange occurred when a test and set instruction (0034*jk*) was holding issue in the next instruction parcel (NIP) register area.

Concurrent Block Writes Bit

When the concurrent block writes (CBW) bit is set in the exchange package, the CRAY Y-MP EL system can have more than one write port active at one time. The CBW bit is specific to the CRAY Y-MP EL system, and is the first mainframe that allows more than one write port to memory. When used, the 002604 instruction enables and the 002504 instruction disables CBW.

Scalar Block Overlap Bit

The scalar block overlap (SBO) bit is another exchange package bit causing a CRAY Y-MP EL system specific function. The function of the SBO is to allow scalar memory references to intermix with memory block references. The 002606 instruction enables SBO, and the 002506 instruction disables SBO.

The remainder of the fields in the exchange package are definitions of the interrupt flags that are set in the exchange package if an exchange sequence is initiated by one of the interrupts, and the mode bits that are user selectable to define program execution. The contents of the A registers and the S registers are also shown in the exchange package.

Exchange

The purpose of the exchange mechanism in the CRAY Y-MP EL system is to provide a means of switching program execution between different programs.

The exchange sequence provides a process in which the currently executing program is gracefully deactivated, with its current operating parameters placed in memory for later retrieval. The next step in the process retrieves the operating parameters of the new program from a specified memory location and places these parameters into the CPU operating registers. The CPU operating registers that are used to contain operating parameters are referred to as the exchange registers, and are spread across several ASICs on the CPU module.

There are a limited number of situations that can cause an exchange to occur, which are:

- Deadstart
- Normal program exit
- Error program exit
- Interrupt

The deadstart sequence starts a program after a power-off/power-on operation or if the operating system is initialized in the mainframe. When these situations occur, the contents of all control latches, words in memory, and all registers are considered invalid.

The mainframe is deadstarted through the IOS 0 maintenance channel, which connects CPU 0 to the IOBB in IOS 0. When a multiple-CPU system is initialized, the deadstart sequence can only occur in one CPU because only one CPU can exchange to memory location 0 at one time. The remaining CPUs in the system must wait for an interrupt from internal CPU (ICP) before they can exchange to memory location 0.

The sequence of events that take place during a deadstart exchange are as follows:

1. Using the scan path, set the following registers and flags:
   - XA = 0
   - MM = 0
   - P = 000000
   - NIP = 001000
   - IBxV = 0
   - NIPVLD = 0 (next instruction parcel valid)
   - HLDISS = 1 (hold issue)
   - All data channels ready to write memory

2. Write 006000 000000 000000 000000 to memory location 0.

3. For each CPU, the console sends a CPURUN ON (010000) command; CPUs will do IFETCH to location 0 and loop on the 006000 instruction.

4. Load the operating system and initial exchange package to location 0 from the IOS using any data channel.

5. Deadstart the first CPU (for example, CPU 0) by sending MCURUPT to that CPU.

6. While CPUs 1 through 3 remain in an idle state, CPU 0 exchanges to location 0.

7. When CPU 0 completes the initial exchange and becomes active, it reloads another exchange package at location 0 and sends an ICP interrupt to one of the idle CPUs, allowing that CPU to exchange to location 0 and become active.

8. The previous 2 steps are repeated until all CPUs in the system are active and able to perform.

NOTE: The CPUs can be deadstarted in any sequence.

Each exchange package resides in an area that is defined during initial system deadstart. This defined area must reside in the lower 4096 (10000_8) words of memory. The exchange package at memory location 0 is the deadstart monitor's exchange package. Only this monitor has an area defined so that it can access all of memory, including other exchange package areas. This area allows the monitor to define or alter all exchange packages other than its own when it is the active exchange package. Other exchange packages provide for objective programs and other monitor tasks and are located outside of the programs' instruction and data areas.

There are also two exit instructions that can initiate an exchange sequence. They are the error exit instruction (000000) and the normal exit instruction (004000). These two instructions are provided so a program can request its own termination. The normal exit instruction allows a program to exchange back to the monitor area. The error exit instruction is used if an abnormal condition is detected by the object program. In this case, the program can exchange to an error handling program at a location specified by the XA field of the exchange package.

The final condition that can cause an exchange is the instance when an interrupt is received by the object program. When this occurs, the object program exchanges with another program at the address specified by the XA field of the exchange package.

Fetch

Any exchange sequence is immediately followed by an instruction fetch operation (a fetch), which reads program code from memory and places it in an instruction buffer. The instruction buffers hold the program code until the code is required by the execution sequence. When needed, the program code is moved from the instruction buffers into the CPU's issue registers.

The CRAY Y-MP EL system uses a P register to initiate a fetch sequence and eight instruction buffers to store the program code. Figure 2-5 shows the relationship between the P register, the instruction buffers, and central memory.

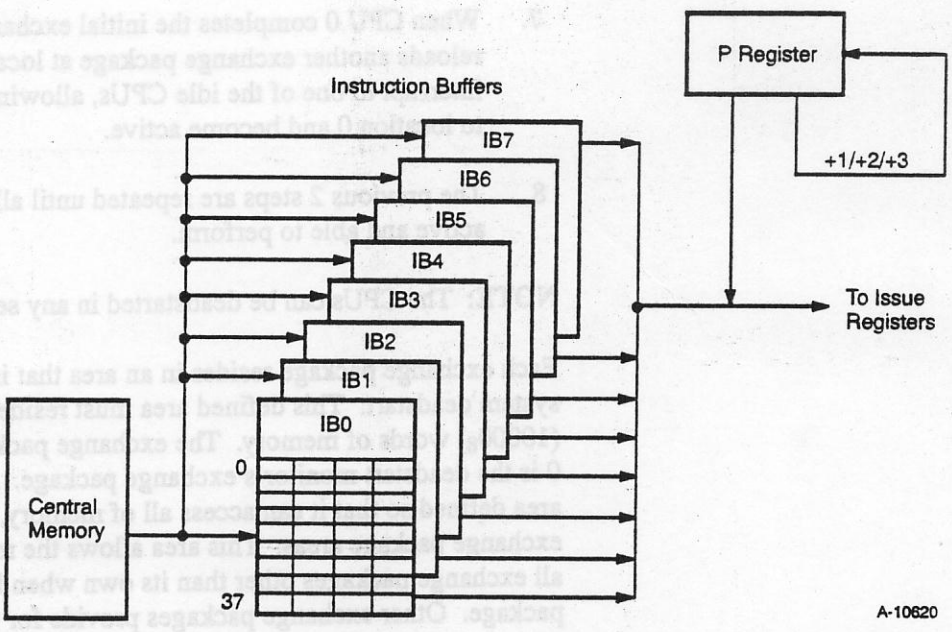

Figure 2-5. Instruction Fetch Hardware

The eight instruction buffers used by the CRAY Y-MP EL system can each hold 40_8 (00 through 37_8) words. Each of these 40_8 words is composed of four 16-bit instruction parcels, providing a total content of 128 parcels. These instruction parcels are held in the instruction buffer until they are selected by the P register to be moved into the issue registers.

The first instruction in an instruction buffer always has a word address that is a multiple of 40_8. This word address allows the entire area of addresses for a single buffer to be defined by the upper 17 bits of the P register.

Each of the instruction buffers has an associated instruction buffer address register (IBAR). The IBAR contains the upper 17 bits of the P register and an IBAR valid bit. When set, the IBAR valid bit is used to indicate that the instruction buffer contains valid data. During an exchange sequence, the IBAR valid bit is cleared, which invalidates the previous program's instructions. When there are no IBAR valid bits set, an instruction fetch sequence is initiated. Note that this condition can occur during normal program execution as well as during an exchange sequence. Once the fetch sequence begins, when instructions are newly loaded into an instruction buffer, the IBAR is loaded with the upper 17 bits of the P register and the IBAR valid bit is set.

The 24-bit P register contains the address of the next parcel of program code that is to enter the NIP register. The upper 22 bits of the P register, shown in Figure 2-6, are used to indicate the word address, while the lower 2 bits are used as parcel select.

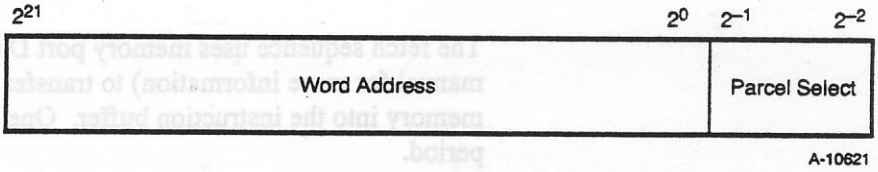

Figure 2-6. P Register

Under normal circumstances, the P register increments sequentially through the program code. This increment occurs whenever an instruction moves into the issue hardware. For a 1-parcel instruction, the P register increments by +1; a 2-parcel instruction causes a +2 increment and a 3-parcel instruction results in a +3 increment. This sequence allows all instructions to issue in 1 clock period. Branch instructions, when encountered, load the P register with the word address of the jump, allowing the program to continue. This branch can occur to another address contained in the instruction buffers, which then issues as if there were no abrupt change. However, it is also possible to issue a branch word address that is not currently held in the instruction buffers. In this instance, a fetch sequence must occur before program execution can continue.

When a program exchanges out, the P register field contains the word address of the instruction immediately following the address of the instruction that last executed.

Instruction Fetch Operation

An instruction fetch operation, or fetch, refers to the series of steps that are performed to read program code from memory into the instruction buffers.

The P register always contains the parcel address of the next instruction that is to be decoded (moved into issue). The decision to fetch is based on the comparison of the P register contents against the contents of the eight IBARs. This comparison check is done each clock period. If the contents of any one of the IBARs is equal to the upper 17 bits in the P register and the IBAR valid bit is set, a condition called in-buffer or coincidence exists and no fetch is required.

If the upper 17 bits of the P register do not match any IBAR, or the IBAR valid bit is not set, a condition called out-of-buffer or no coincidence exists. In this condition, there are no valid instructions in the instruction buffers and a fetch sequence is initiated.

The fetch sequence uses memory port D (refer to Section 3 of this manual for more information) to transfer 128 parcels (40_8 words) from memory into the instruction buffer. One word is transferred each clock period.

The instruction buffers are circularly loaded. This means that a fetch sequence moves 128 parcels into the first instruction buffer, then another fetch is required to fill the next instruction buffer. This process continues sequentially until all eight instruction buffers are filled or until the ILA is reached. If a program requires more than 1024 parcels (eight fetch sequences), the ninth fetch operation overwrites the first instruction buffer used.

The first word delivered to the instruction buffer always contains the instruction that is the first instruction to be executed. As an example, if the P register contained the address 124-2 (parcel 2 of word 124), when the fetch operation started, the first word delivered to the instruction buffer will be from memory address 124.

During an instruction fetch operation, instructions are delivered to the instruction buffer at a rate of one instruction per clock period. Because of overhead, it takes 16 clock periods for the first word to arrive from memory, and an additional 2 clock periods for the first instruction to get to the NIP register. Instruction issue can occur concurrently with the fetch operation as long as the required instruction parcel is in the instruction buffer. As long as no memory conflict occurs, an instruction buffer can be loaded in 47 clock periods. However, memory conflicts can lengthen the time required to complete a fetch.

Instruction Issue

The CRAY Y-MP EL system makes use of three different registers as parts of the instruction issue hardware. Figure 2-7 shows the registers used, the instruction buffers, and the general flow of the instruction parcels as they move into execution.

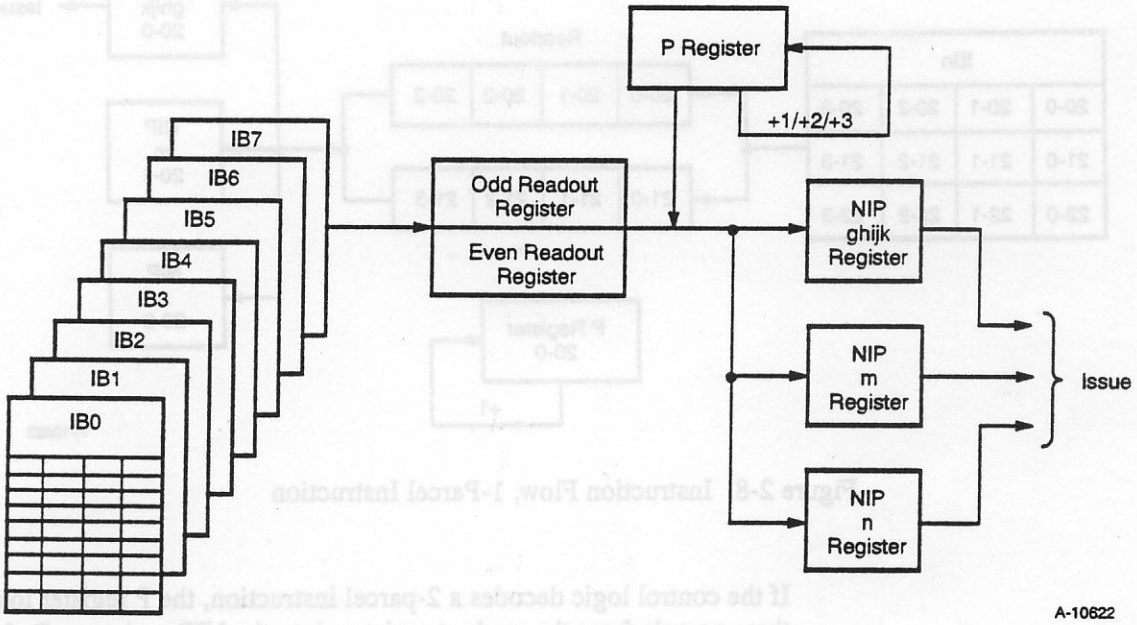

Figure 2-7. Instruction Issue

The instruction buffers hold the program code read from memory until it is moved to the issue registers. The instruction buffers have two associated readout registers that are used to channel the flow of instructions between the instruction buffers and the next instruction parcel (NIP) registers. Even-numbered words are loaded into the even readout register, while odd-numbered words move to the odd readout register. Bit 2^0 of the P register determines which readout register to use, while bit 2^{-1} and bit 2^{-2} select the parcel that is to be sent to the NIP registers. The readout registers contain eight parcels (four even parcels and four odd parcels).

The P register value addresses the instruction buffer and moves three instruction parcels into NIPghijk, NIPm, and NIPn. These three parcels are selected from the eight available in the readout registers. At the same time the three parcels are gated into the NIP registers, the type of instruction is determined (1-, 2-, or 3-parcel) and the appropriate add (+1, +2, +3, or -1) is performed on the P register. When this add is complete, the next instruction is selected and moved into the readout registers. The cycle continues until the program terminates.

In the case of a 1-parcel instruction, the P register gates three parcels into the NIP registers. Refer to Figure 2-8. The first parcel enters register NIPghijk, the second parcel goes to register NIPm, and the third parcel enters register NIPn. If there are no conflicts, the instruction parcel located in register NIPghijk issues and the P register increments by +1.

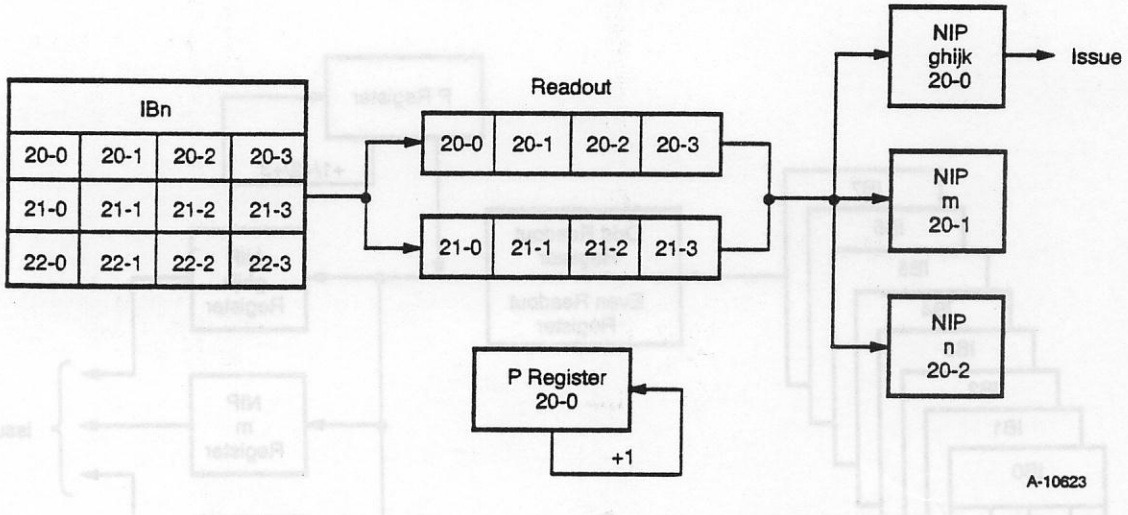

Figure 2-8. Instruction Flow, 1-Parcel Instruction

If the control logic decodes a 2-parcel instruction, the P register loads three parcels from the readout registers into the NIP registers. Refer to Figure 2-9. As with a 1-parcel instruction, the first parcel enters register NIPghijk, the second parcel enters register NIPm, and the third parcel is placed in register NIPn. If there are no conflicts, the parcels placed in register NIPghijk and register NIPm are issued, and the P register increments by +2.

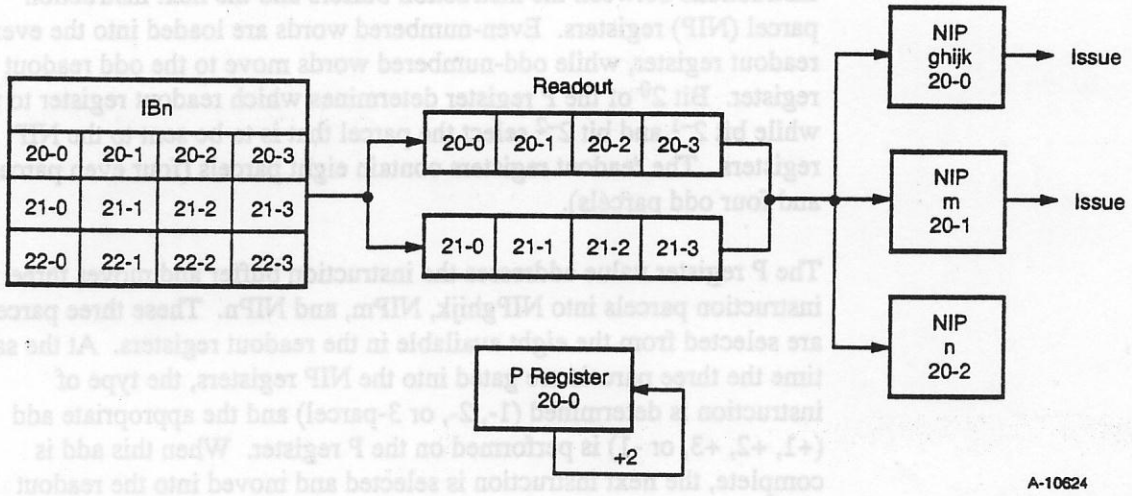

Figure 2-9. Instruction Flow, 2-Parcel Instruction

When a 3-parcel instruction is presented to the control logic, the NIP registers are loaded as indicated above. However, when the instruction moves into issue, all three NIP registers are used and the P register increments by +3. Refer to Figure 2-10.

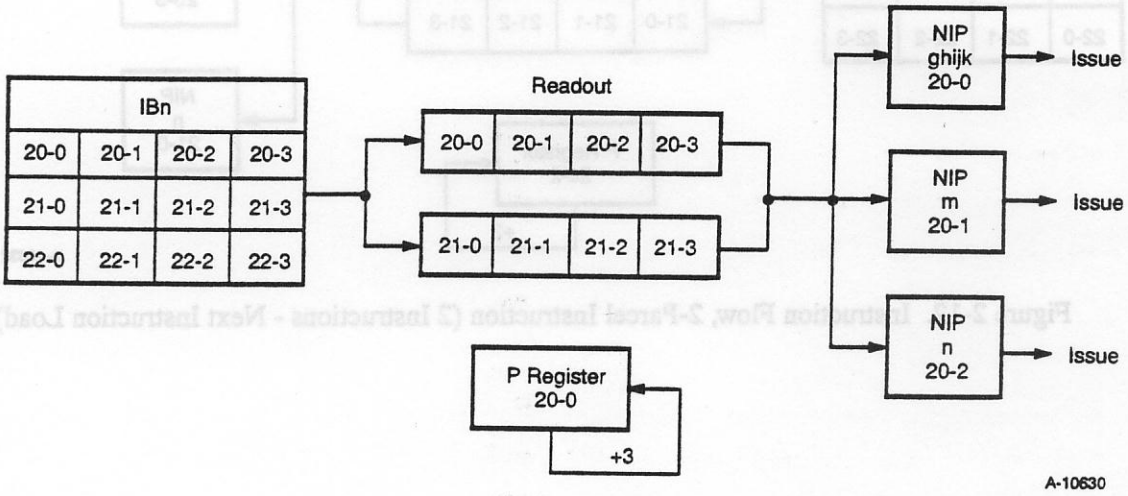

Figure 2-10. Instruction Flow, 3-Parcel Instruction

Any unused instruction parcel remaining in one of the NIP registers is overwritten during the next instruction load sequence, rather than using time to clear the NIP registers before reloading them. Refer to Figure 2-11, Figure 2-12, Figure 2-13, and Figure 2-14 for more information.

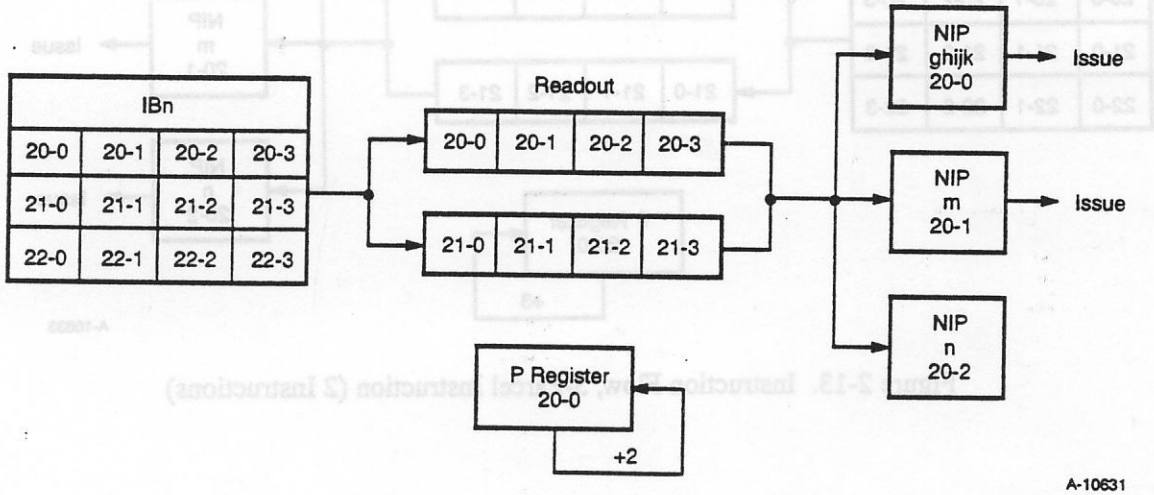

Figure 2-11. Instruction Flow, 2-Parcel Instruction (2 Instructions)

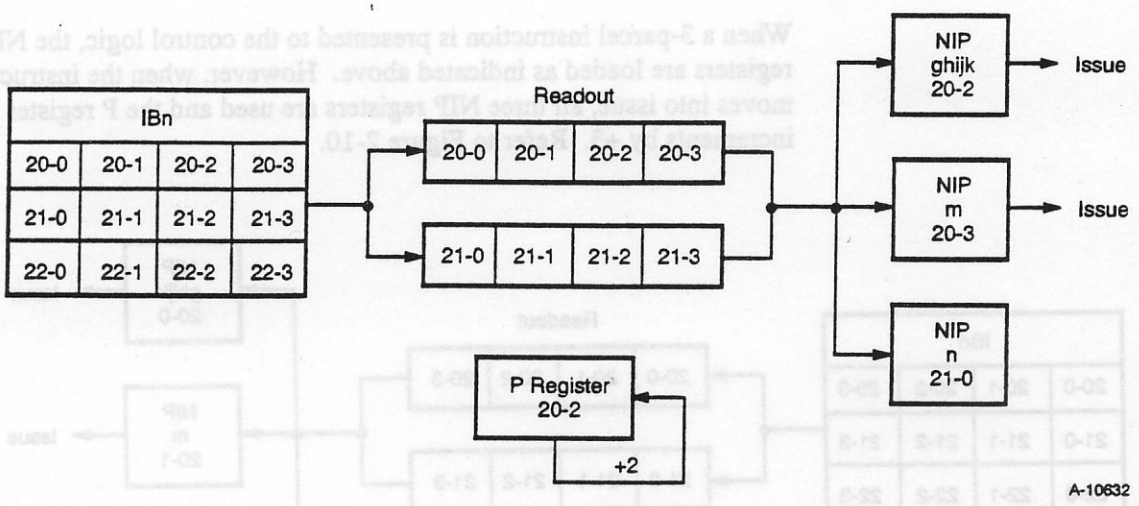

Figure 2-12. Instruction Flow, 2-Parcel Instruction (2 Instructions - Next Instruction Load)

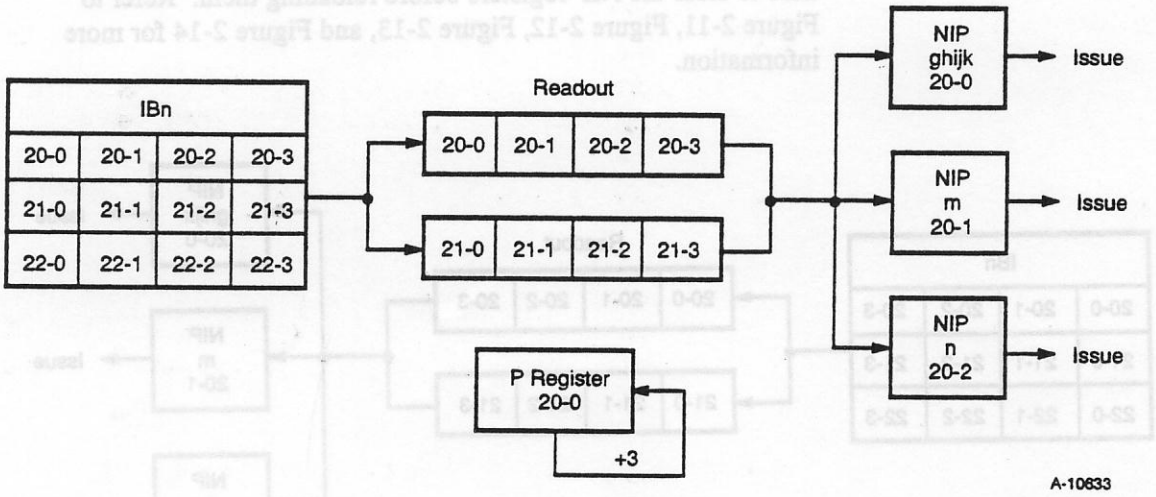

Figure 2-13. Instruction Flow, 3-Parcel Instruction (2 Instructions)

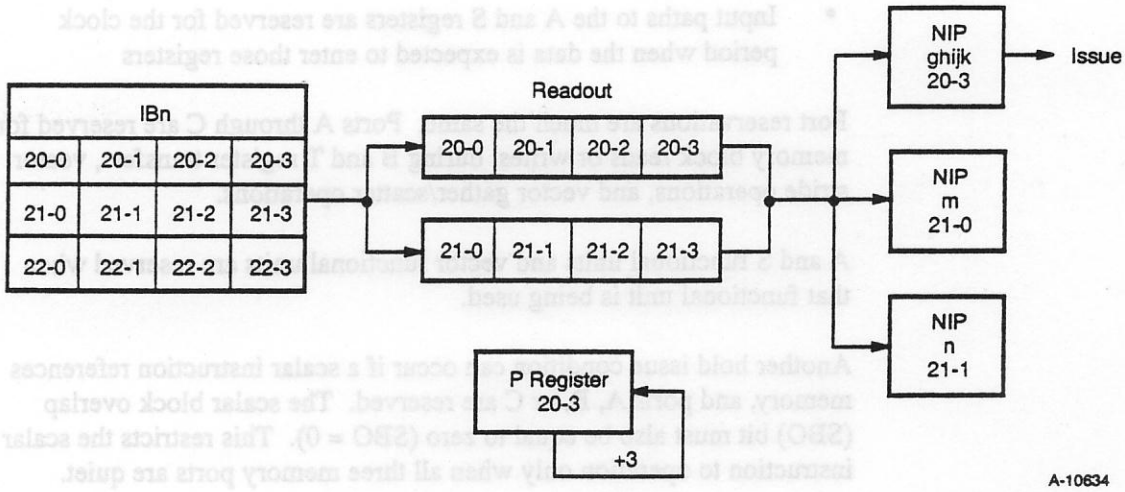

Figure 2-14. Instruction Flow, 3-Parcel Instruction (2 Instructions - Next Instruction Load)

Instructions continue to flow through the issue registers until the program code exits normally or is interrupted. In either case, an exchange and fetch operation brings new code into the instruction buffers and a new value into the P register, and the issue sequence starts again. As long as there are instructions in the instruction buffers and there are no conflicts, the CRAY Y-MP EL system can issue a 1-, 2-, or 3-parcel instruction every clock period.

Reservations and Hold Issue Conditions

When an instruction is in the NIP registers, hardware checks are made to determine whether there are any conflicts that would prevent the instruction from completing. These conflicts are referred to as hold issue conditions, because they cause the instruction to be held in the NIP registers until the conflict condition is resolved. Once an instruction issues, reservations are immediately placed on the appropriate registers, paths, ports, or functional units required for the completion of that instruction. These reservations are held until a Reset signal is received from the appropriate resource indicating that the instruction has finished using that resource.

The conditions that cause registers to be reserved are:

- A and S registers are used as result registers
- B and T registers are used during block transfers
- V registers are reserved as either operand or result registers

- Input paths to the A and S registers are reserved for the clock period when the data is expected to enter those registers

Port reservations are much the same. Ports A through C are reserved for memory block reads or writes, during B and T register transfers, vector stride operations, and vector gather/scatter operations.

A and S functional units and vector functional units are reserved when that functional unit is being used.

Another hold issue condition can occur if a scalar instruction references memory, and ports A, B, or C are reserved. The scalar block overlap (SBO) bit must also be equal to zero (SBO = 0). This restricts the scalar instruction to operation only when all three memory ports are quiet.

When using multiple parcel instructions, it is possible to have a 2-clock-period hold issue condition if the second or third parcel of the instruction is in a different instruction buffer. If the second or third parcel is not in any of the instruction buffers, a fetch operation is performed, which requires 47 clock periods to complete.

Interprocessor Communications

Interprocessor communications on the CRAY Y-MP EL system pass data and control between CPUs. There are three elements of interprocessor communications used by the CRAY Y-MP EL system:

- Shared registers
- Semaphore registers
- Interprocessor interrupts

The purpose of the shared registers is to pass data between the CPUs. The semaphore registers synchronize the operation of a program among CPUs. The interprocessor interrupts allow one CPU to initiate an exchange sequence in a different CPU. Together, these three functions are especially useful when the CRAY Y-MP EL system is used in a multitasking environment.

The shared registers and the semaphore registers are arranged into groups, called clusters, on the CPU.

Clusters

The CRAY Y-MP EL system contains the shared registers and the semaphore registers into seven clusters on each CPU. A CPU may access only one cluster at a time. The cluster number (CLN) register in the exchange package determines which cluster the CPU has access to in

the specific program being run. The clusters are numbered 1 through 7. A CLN = 0 condition is used to prevent a CPU from accessing the shared registers. This function can be used to reserve a CPU in single-user mode for a specific program.

There are two ways to change the contents of the CLN register in the CRAY Y-MP EL system. One way is an exchange (refer to the Exchange subsection in this section). A second way requires the CPU to be in monitor mode and executing an 0014*j*3 instruction. (Refer to Appendix A for details pertaining to the CRAY Y-MP EL system instruction set.)

Shared Registers

Shared registers are used to transfer data among operating registers in different CPUs. The CPU being used by a program can load its shared registers from its own operating registers. A different CPU (or several different CPUs) can then transfer this data into their shared registers, and then transfer the data from the shared registers into its operating registers. This function occurs only if the involved CPUs are all operating in the same cluster.

The CRAY Y-MP EL system contains two types of shared registers: the shared address (SB) registers and the shared scalar (ST) registers. Each cluster contains eight 32-bit SB registers, numbered SB0 through SB7, and eight 64-bit ST registers, numbered ST0 through ST7. There are four instructions associated with transferring data between the operating registers and the shared registers in a cluster of a single CPU:

- 026*ij*0 Transmit (SB*j*) to A*i*
- 027*ij*7 Transmit (A*i*) to SB*j*
- 072*ij*3 Transmit (ST*j*) to S*i*
- 073*ij*3 Transmit (S*i*) to ST*j*

If CLN = 0 when the CPU exchange package issues these instructions, the 026 and 072 instructions return a 0 to the designated registers, while the 027 and 073 instructions do not perform any operation.

Semaphore Registers

The semaphore (SM) registers enable a CPU to temporarily suspend operation of a program to allow synchronization of that CPU with other CPUs. Each cluster in a CPU contains 32_{10} 1-bit SM registers, numbered SM0 through $SM37_8$. During program execution, each CPU assigned to a specific operating cluster sets and clears all SM registers

within that cluster. Each of the CPUs assigned to the cluster can also transmit the contents of the SM registers to or from an S register for examination.

There are five instructions used by the SM registers:

- 0034*jk* Test and set semaphore *jk*
- 0036*jk* Clear semaphore *jk*
- 0037*jk* Set semaphore *jk*
- 072*i*02 Transmit (SM) to S*i*
- 073*i*02 Transmit (S*i*) to SM

The 0034 instruction tests the state of the semaphore register specified in the *jk* field. If the content of the SMjk register is 0, the instruction executes immediately. If the content of SMjk is 1, the 0034 instruction holds issue until another CPU assigned to the same cluster clears the SMjk register. When the 0034 instruction issues in either of these cases, it sets the SMjk register to 1.

Instructions 072 and 073 are used to transfer the contents of the semaphore registers to or from the upper 32 bits of the designated S register. The relationship between the registers involved in this transfer is shown in Figure 2-15. The contents of SM0 are transferred to bit position 2^{63} of the S register, while the contents of SM37 are placed in bit position 2^{32}. The lower 32 bits of the selected S register are unused during this type of transfer.

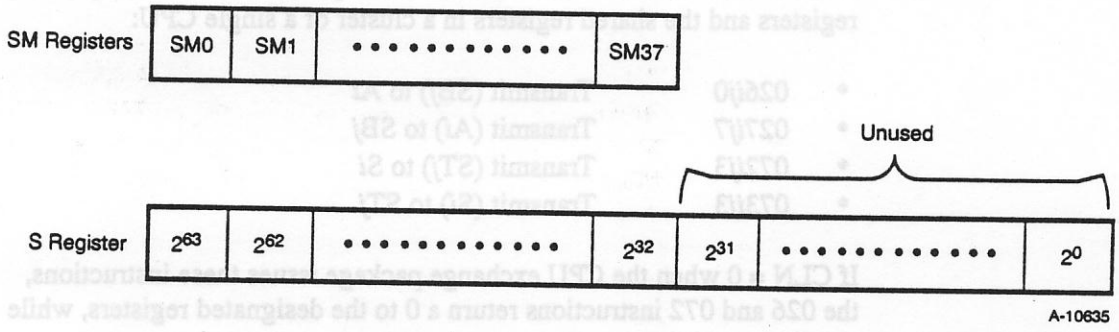

Figure 2-15. Relationship between Semaphore Registers and an S Register

Deadlock

A deadlock is a condition that occurs when all CPUs assigned to a cluster are holding issue on an 0034*jk* (test and set) instruction. If this condition exists, no program execution can occur in any of the CPUs assigned to the cluster because each is waiting for one of the others to issue a clear SM (0036*jk*) instruction.

A deadlock interrupt resolves a deadlock condition. Then, in each of the CPUs where the interrupt occurred, the deadlock (DL) flag sets in the exchange package. This causes each of the deadlocked CPUs to execute an exchange sequence, clearing the deadlock.

Two special conditions can occur regarding a deadlock condition. First, if a CPU has a CLN = 0, a deadlock condition cannot occur because the 0034 instruction should perform no operation. If a DL flag is continuously being set, and the program is being denied execution because of this, it could be advantageous to test the 0034 instruction in an offline environment to help isolate the error.

The second condition involving a deadlock occurs only if one CPU is assigned to a specific cluster. In this case, the CPU encounters a deadlock if it issues an 0034 instruction. There is no other CPU available to clear that set condition.

Interprocessor Interrupts

The final segment of interprocessor communications involves interprocessor interrupts, which occur when a CPU interrupts another CPU's program. A CPU must be in monitor mode to issue the interrupt instructions. The interrupt instructions are:

- 0014*j*1 Set interprocessor interrupt request of CPU (A*j*)
- 001402 Clear interprocessor interrupt request

When the 0014*j*1 instruction is executed, the interrupt from internal CPU (ICP) flag is set in the CPU specified by (A*j*). If this CPU is not in monitor mode, it begins an exchange sequence. The program that enters the CPU is in monitor mode and issues a 001402 instruction, clearing the ICP flag. If this instruction does not execute, the CPU immediately begins another exchange sequence.

In a special case, the 0014*j*1 instruction is executed with the contents of Aj equal to the number of the CPU executing the instruction (the CPU is, in effect, interrupting itself), no operation is performed.

Real-time Clock

The CRAY Y-MP EL system has a device called the real-time clock (RTC). The RTC consists of four identical devices, one on each CPU, running synchronously to appear as one RTC to the programmer. In this discussion, the combination of circuits forming the actual RTC will be treated as a single device, since a mainframe containing only one CPU (one RTC device) performs the same as a mainframe containing four CPUs (four RTC devices).

The RTC is a 64-bit register that increments each clock period. Two instructions affect the RTC:

- 0014*j*0 Transmit (S*i*) to RTC
- 072*i*00 Transmit (RTC) to S*i*

The 0014*j*0 instruction can be executed by a CPU that is in monitor mode only. Two or more CPUs in monitor mode should not attempt to execute this instruction simultaneously as unpredictable results will occur. However, there is no hardware to detect this situation. The 072*i*00 instruction can be executed simultaneously by any number of CPUs, because only the copy of the RTC on the local CPU is read to the S register.

3 MEMORY

The memory portion of the CRAY Y-MP EL computer system consists of four modules. These modules currently are provided in two types: a fully populated module and a half-populated module. Both module types are constructed on 16 x 22 x .093 inch printed circuit (PC) boards consisting of 16 circuit layers. The 16 layers are:

- 1 top pad
- 1 bottom pad
- 4 ground (Vss) layers
- 4 power layers: 5-volt application-specific integrated circuit (ASIC); 6-volt dynamic random access memory (DRAM)
- 6 signal layers

The logic portion of a memory PC board comprises two types of application specific integrated circuits (ASICs) and a group of DRAM chips. There are nine ASICs on each memory board: two memory array control (MAC) ASICs and seven memory array data (MAD) ASICs. The number of DRAM chips on each memory PC board is determined by the memory size selected by the customer. Currently, the CRAY Y-MP EL system can be supplied with either a 32-Mword memory, a 64-Mword memory, or a 128-Mword memory.

The 32-Mword and 64-Mword memory options are half-populated memory boards that contain 288 DRAM chips. Each of these DRAM chips is a 1M x 4 memory chip with a 70 nanosecond (ns) access time. The same DRAM chip is used with the 128-Mword memory, but there are 576 memory chips mounted on the fully populated memory board. Refer to Figure 3-1 for a diagram of a fully populated memory module.

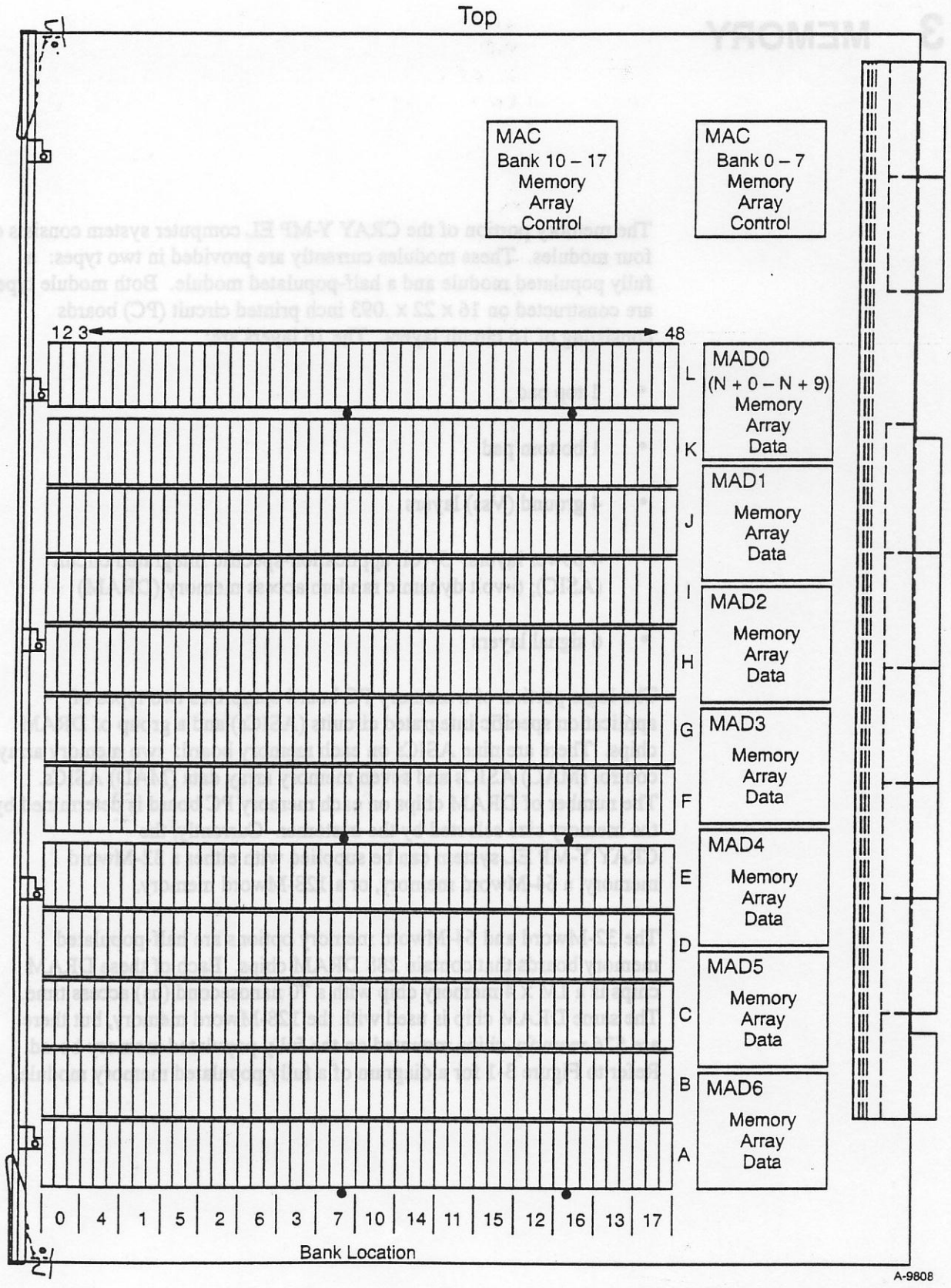

Figure 3-1. Fully Populated Memory Module

Memory is divided into 16 banks for addressing whether the module is half-populated or fully populated. The fully populated module contains an upper 16 banks and a lower 16 banks of addressable memory; the half-populated module uses only the lower 16 banks. The difference between the 32-Mword and the 64-Mword memory modules is that there is one extra address bit enabled on the 64-Mword modules.

Because there are 16 banks of memory on each memory module, the mainframe has a total of 64 banks of memory. The memory is also separated into sections; each memory module is one section. This arrangement provides the mainframe with four memory sections, each consisting of 16 banks.

The CRAY Y-MP EL system uses a 32-bit address scheme, of which 27 bits (0 through 26) are used. The bits are assigned as shown in Figure 3-2. Bits 2^0 and 2^1 are used to select the appropriate section and bits 2^2 through 2^5 are used for bank selection.

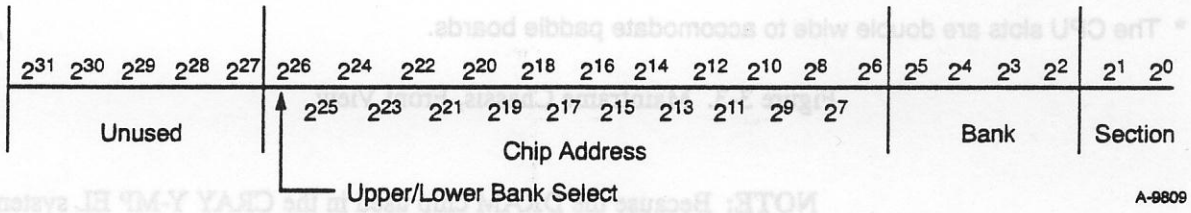

Figure 3-2. Address Bit Assignments

The remainder of the address bits, with one exception, are used to select the actual memory location. The exception is bit 2^{26}, which is used as the upper/lower bank select bit. This bit is only necessary on a fully populated 128-Mword memory module. The internal addressing scheme, represented by bits 2^6 through 2^{25}, uses a row and column scheme. The odd-numbered bits are used to count the rows of memory, while the even-numbered bits are used to locate the column. To determine the failing memory module decode bits 2^0 and 2^1 to determine which section is in error. This corresponds to a specific memory module. The locations of the memory sections is shown in Figure 3-3, a representation of the eight-slot mainframe card cage. All of the memory modules are interchangeable, so swapping the suspected failing module with a good module can help isolate the failure.

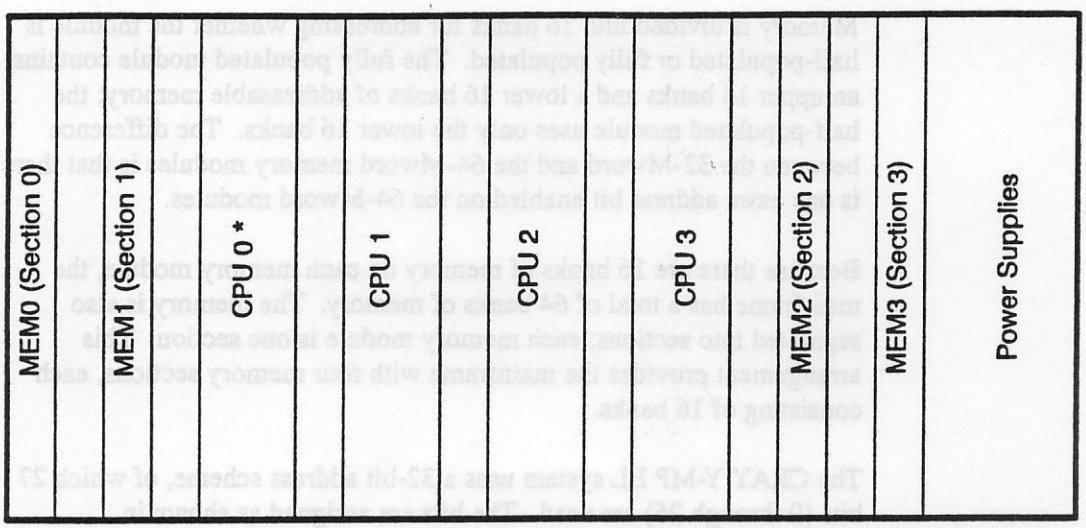

Figure 3-3. Mainframe Chassis, Front View

NOTE: Because the DRAM chip used in the CRAY Y-MP EL system memory is a 1M x 4 chip, it is expected that a single-bit error will rapidly escalate into a multiple-bit error. For this reason, it is important to repair single-bit errors as soon as possible.

Other specifications of the DRAM chip are:

- ZIP package .4 x 1.03 inch
- 5 clock period bank access time
- Standby power = 5 milliwatts at 5 volts
- Active power = 550 milliwatts at 5 volts

The rest of the memory PC board is made up of two types of MAC and MAD ASICs. The MAC ASIC chip supports four memory operations:

- Read, a normal DRAM read operation, lasts 5 clock periods.
- Write, a normal DRAM write operation, lasts 5 clock periods.
- Refresh, which uses row address strobe (RAS) to refresh data, lasts 5 clock periods.

- Read/Modify/Write (RMW) is used during an exchange, and uses normal DRAM read operations followed by a normal DRAM write operation to the same address. RMW lasts 10 clock periods.

The refresh control for the DRAM chips is located on the CPU and memory PC boards.

Other functions of the MAC ASIC include:

- Connects any of the four processors to any of the 16 banks through an address crossbar
- Controls both address and control signals
- Holds a refresh address counter
- Controls all of the MAD ASICs

The MAD ASICs perform the following functions:

- Each handles a specific portion of the 72-bit memory data word
- Each contains a data crossbar which connects any of the four processors to any of the 16 banks

The interconnection between the MAD, MAC, and DRAM chips is represented in Figure 3-4. Note that MAC 0 controls operations for banks 0 through 7, and MAC 1 controls banks 10 through 17. The content of the entire data bus is presented to the seven MAD ASICs and each receives its assigned bits. The bits assigned to each MAD ASIC are in no specific order. If a random group of bits of data are reported as failing, it could in fact be a single MAD that is failing.

NOTE: When an ASIC fails, the failing chip is removed from the PC board, discarded, and replaced by a new ASIC. No internal repairs are possible. Therefore, field repair to the ASIC level is not allowed. Instead, remove and replace the memory module containing the failing ASIC.

Other important characteristics of CRAY Y-MP EL system memory modules are:

- Each memory module contains 8 Mwords or 16 Mwords of memory if half-populated and 32 Mwords if fully populated
- Operates with a 30-ns clock period
- Air cooled

- Connected to the backplane by two types of connectors:

  120 pins x 7 connectors = 840 pins
  90 pins x 1 connector = 90 pins
  930 pins

- Connected to the individual CPUs using four ports per CPU; all ports are read/write ports

- There is no hardware error logger. Single- and double-bit errors are reported to the operating system and stored in error files.

- 270 watts per module = 1080 watts per system

- Voltage = + 6 volts

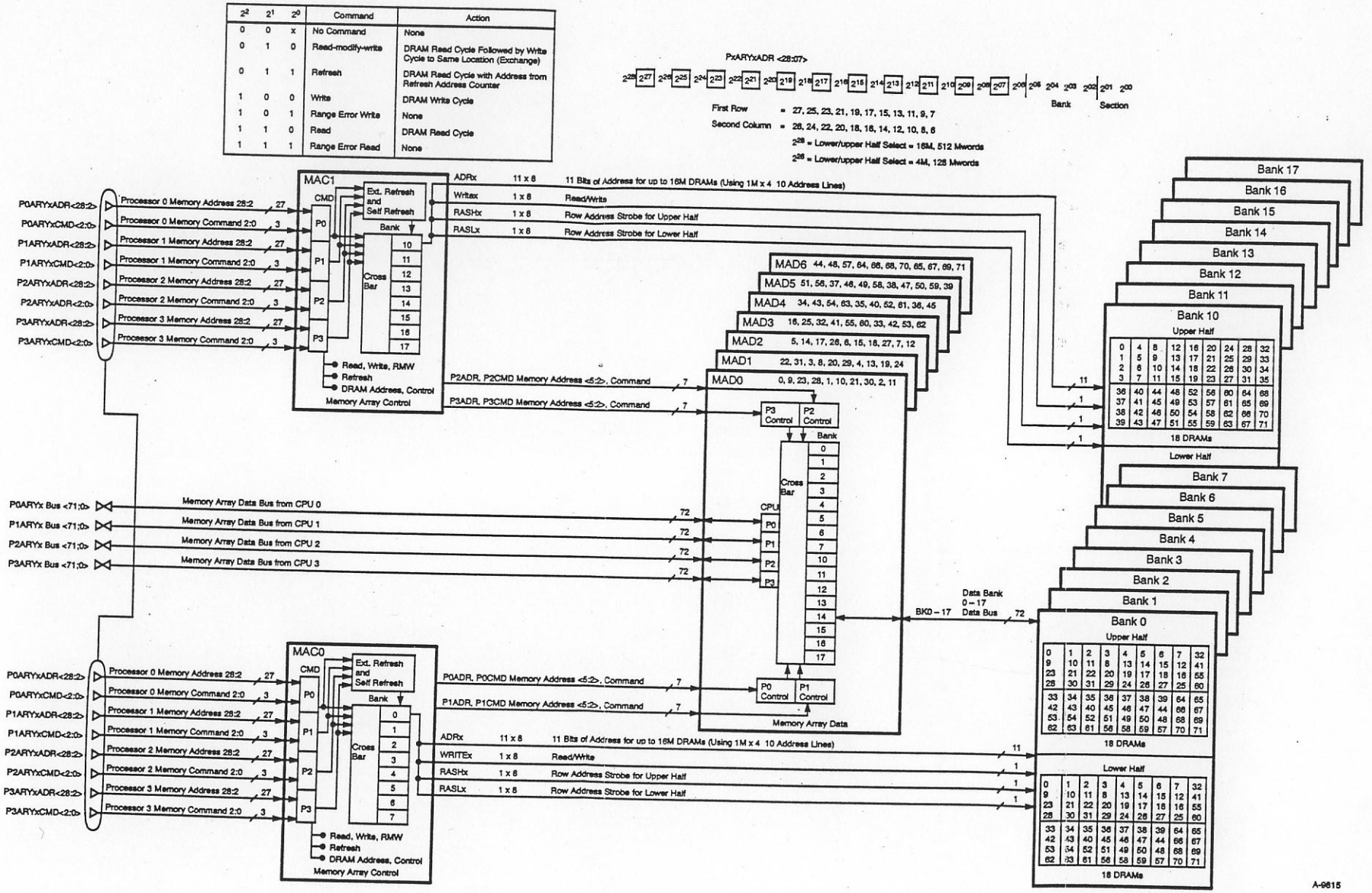

Figure 3-4. Memory Block Diagram

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Memory Organization

Figure 3-5 shows the major architectural features of the CRAY Y-MP EL system memory. As shown, memory is divided into four sections, each containing 16 banks. This enables simultaneous memory references (two or more memory references that begin in the same clock period) and overlapping memory references (one or more memory references that begin while another reference is in progress).

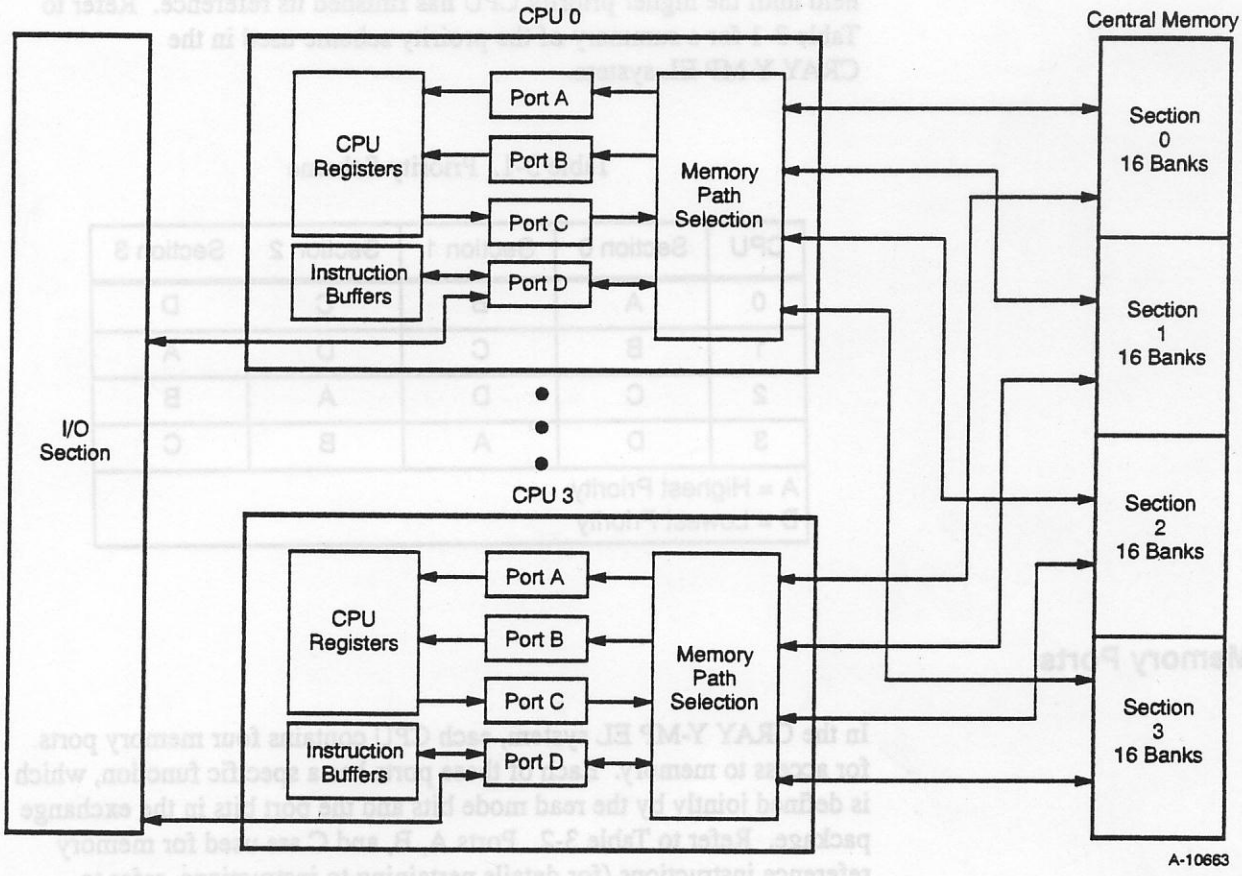


Figure 3-5. Central Memory Architecture

Memory Paths

Each CPU in the CRAY Y-MP EL system has an independent path into each of the memory sections. This allows a CPU to make up to four simultaneous memory references, one to each section. Overlapping memory references are allowed to different sections without any restrictions. Likewise, overlapping memory references are allowed to the same memory section as long as each reference uses a different bank of memory. Because each CPU only has one path into each section of

memory, simultaneous memory references to the same section are not allowed, and one reference is forced to hold until the other reference completes.

Simultaneous and overlapping memory references from two or more CPUs are subject to fewer restrictions. These memory references are allowed to one section of memory. The only restriction is that each reference must use a different bank. If a simultaneous or overlapping memory reference require the same bank, a priority definition is made between the requesting CPUs. The CPU with the lowest priority is then held until the higher priority CPU has finished its reference. Refer to Table 3-1 for a summary of the proirity scheme used in the CRAY Y-MP EL system.

Table 3-1. Priority Scheme

CPU	Section 0	Section 1	Section 2	Section 3
0	A	B	C	D
1	B	C	D	A
2	C	D	A	B
3	D	A	B	C
A = Highest Priority D = Lowest Priority				

Memory Ports

In the CRAY Y-MP EL system, each CPU contains four memory ports for access to memory. Each of these ports has a specific function, which is defined jointly by the read mode bits and the port bits in the exchange package. Refer to Table 3-2. Ports A, B, and C are used for memory reference instructions (for details pertaining to instructions, refer to Appendix A). Port D is shared by the instruction buffers in the CPU and by the I/O section. All four ports are used for exchange operations and for refresh functions.

Table 3-2. Port and Read Mode Field Translation

Port Bits (P)								Read Mode Bits (RM)				Port Usage
6 1	6 0	6 1	6 0	6 1	6 0	6 1	6 0	5 9	5 8	5 7	5 6	
A 0	0	B 0	1	C 1	0	D 1	1	0	0	0	1	Exchange
0	0	0	1	1	0	–	–	0	0	1	0	A or S
–	–	–	–	–	–	D x	x	0	1	0	1	I/O single
–	–	–	–	–	–	D x	x	0	1	1	1	I/O block
0	0	0	1	1	0	–	–	1	0	0	0	B or T
–	–	–	–	–	–	D x	x	1	0	1	1	Fetch
0	0	0	1	1	0	–	–	1	1	0	0	Vector stride
0	0	0	1	1	0	–	–	1	1	1	0	Vector gather/scatter

Port D normally has a lower priority than ports A, B, and C when it is used for I/O transfers. However, if a memory reference is forced to wait from 0 to 255 clock periods on an I/O transfer, it is given highest priority for one memory reference. When the reference begins, port D is returned to lowest priority. The actual number of clock periods used as a hold figure can be determined using the scan chain capability of the CRAY Y-MP EL system. This function is normally accomplished during the initial software tuning stage.

All of the memory ports are bidirectional. The reservation system makes use of any memory port as it becomes available, but the ports are subject to a priority system. This priority system provides a fetch sequence, with the highest priority on port D; I/O operations are given the lowest port D priority.

Ports A, B, and C operate differently when they are doing block or vector transfers than when a scalar transfer is being performed. When a port becomes available, the instruction issues and reserves the port. That port remains reserved until the instruction completes all of its memory references. After completion of the memory reference, the port reservation is cleared, and the port is available for the next instructions reservation. Under normal circumstances, a block or vector transfer is capable of reading or writing one word of data each clock period. However, if the instruction encounters a memory conflict, it is

suspended, or held, until the conflict is resolved. Because of this, the time needed to complete an instructions block or vector reference is unpredictable.

Block and vector transfers that use different ports are allowed to operate simultaneously, which may cause problems under certain circumstances. For example, if an 035*ijk* instruction precedes a 176*i*0*k* instruction that uses one or more of the same memory addresses, it is possible that some memory addresses could be read before they are written to. This is an out-of-sequence reference.

There are two ways to prevent out-of-sequence references. The first is to use the 002700 instruction, which forces completion of the memory reference. When inserted between the write instruction (035*ijk*) and the read instruction (176*i*0*k*), it forces the selected port to hold issue until the write instruction completes. Secondly, if the bidirectional mode (BDM) bit in the exchange package is clear (BDM = 0), out-of-sequence memory references are prevented. In this case, instructions using a port for a write operation prevent any other port from issuing a read instruction.

A scalar transfer instruction requires that ports A, B, and C be available before it can issue so that block transfers and scalar references within a CPU are sequential. A scalar reference uses one of the available ports, and consecutive scalar references are issued as long as a port is available. A scalar reference always completes in the order in which it was issued within the CPU.

The CRAY Y-MP EL system also has the added features of the concurrent block write (CBW) function and the scalar block overlap (SBO). These bits are part of the exchange package. The SBO allows scalar and block references to intermix, while CBW allows more than one block write to occur at the same time, as long as they are using different ports.

On port D, an instruction fetch sequence has priority over an I/O transfer. If a memory section conflict occurs, port D has priority over all other ports during fetch.

Memory Conflicts

There are several conditions that cause memory conflicts. For example, conflicts occur when a memory port attempts to access a portion of memory that is already busy, or when two or more ports try to access the same portion of memory at the same time. Intra-CPU conflicts involve ports within the same CPU. Inter-CPU conflicts involve ports in different CPUs. In both cases, conflict resolution logic is used to impose a predetermined priority scheme to resolve the conflict.

There are three types of memory conflicts: section, simultaneous bank, and bank busy. Each of these conflicts is resolved differently.

A section conflict is caused when more than one port in the same CPU attempts to access the same memory section simultaneously. Since each CPU has only one path to each memory section, multiple references simultaneously create conflicts. These conflicts are resolved by a priority system among the four ports. The port having the highest priority is granted access to memory first. All other ports attempting a memory reference from that CPU at that time are subjected to a 1-clock-period hold issue condition. The port priority is determined using the following rules:

- Port D has priority over ports A, B, and C during a fetch sequence.
- If a conflict occurs between ports A, B, or C, any port with an odd address increment has priority over an even address increment. An address has an odd or an even increment, depending on the following conditions:
  - A port used for a block reference instruction has an address increment of 1, which is odd.
  - A port used by a stride reference instruction can have any constant increment (even or odd).
  - A port used by a gather/scatter instruction can have an increment that changes after each reference. For conflict resolution, a gather/scatter instruction always has an odd increment.
- Among ports A, B, and C, if all have the same type of memory increment, priority is determined by the relative time of instruction issue. The port used by the instruction issued first has the highest priority.
- Port D has the lowest priority when used for I/O transfers.

A simultaneous bank conflict occurs when two or more ports in different CPUs attempt to access the same bank in a memory section at the same time. The CPU assigned the highest priority is allowed to access the bank first, and all other CPUs are held for 1 clock period. Refer to Table 3-1. Following a simultaneous bank conflict, each port that was held encounters a bank busy memory conflict.

The bank busy conflict occurs because each memory reference by a CPU holds that memory bank busy to all ports in all CPUs for 5 clock periods. The bank busy then occurs if any port in another CPU tries to make a memory reference to the same bank during this 5 clock periods. The

new memory reference holds for 1 to 4 clock periods until the old reference is no longer holding the bank busy. If other ports try to access a busy memory bank and are forced to hold, they experience a simultaneous bank conflict when the bank busy conflict is resolved.

Memory Access Time

Access time is the time required for an instruction to transfer one or more operands from memory to an operating register. Access time depends on the type of register receiving the operand and the number of operands being transferred. If no memory conflicts are encountered, the access times for each register are:

- 16 clock periods for A registers
- 16 clock periods for S registers
- 16 plus block length clock periods for B and T registers
- 16 plus vector length clock periods for vector register stride references
- 18 plus vector length clock periods for vector register gather references

4 INPUT/OUTPUT SUBSYSTEM

The input/output subsystem (IOS) of the CRAY Y-MP EL computer system acts as a preprocessor and interface between the mainframe section (central processing unit and memory) and the various customer-selected peripheral devices. This section describes devices incorporated within the IOS as well as their functions.

Basic Architecture

The IOS used in the CRAY Y-MP EL system is a VMEbus-based device. This VME is a modular design, and thus is easily adapted to customer requirements. The IOS is available in three different backplane configurations:

- 10 slots + 10 slots
- 10 slots + 6 slots + 4 slots
- 6 slots + 4 slots + 6 slots + 4 slots

Cray Research, Inc. (CRI) uses a VME backplane that supports the double-height 233 mm (6U) x 160 mm printed circuit (PC) board, which fits into a standard 19-inch rack.

The CRAY Y-MP EL system can support up to four independent IOSs for each installed CPU. Thus, a fully enhanced system containing four CPUs can support 16 IOSs. Each of the IOSs communicates with its associated CPU via the Y1 bus, a 40-Mbyte/s channel. Each IOS is powered by a 1000-watt power supply and is air cooled.

IOS 0 is required and must reside in the primary cabinet. This primary IOS, designated the multiplex input/output processor (MIOP), consists of:

- Type 68030-processor based processor board
- Local memory
- Control store

The primary IOS also includes the following devices that are connected to the small computer system interface (SCSI):

- Winchester disk drive
- Cartridge tape drive (0.25-inch)
- Communications port for the operator's console
- Remote diagnostic facility
- Helical-scan tape system

Many peripheral products can be connected to an IOS. Some of these are:

- Networks using TCP/IP
  - HYPERchannel
  - Fiber-distributed device interface (FDDI)
  - Ethernet
- Several varieties of disk drives
- Several varieties of tape drives

For a more detailed list of peripherals supported by the IOS, refer to Section 5 of this manual.

Each of these devices must be driven by a VMEbus-compatible device controller. Cray Research recommends and supports several of these controllers, but the customer may provide other controllers. The IOS backplane can contain up to 8 of these peripheral controllers (in the 10-slot configuration). However, each IOS must contain an I/O processor (IOP) board and a CPU channel communications interface board.

The IOP selected for the CRAY Y-MP EL system IOS is a type 68030-based board supplied by Heurikon Corporation. This IOP supports the SCSI, allows I/O computation, and controls IOS-to-CPU communications. Communication between the IOS and CPU takes place via the IOBB.

Heurikon HK68/V30

The Heurikon HK68/V30 acts as the IOS master controller, handles all of the VMEbus interrupts, acts as a communications arbitrator for the VMEbus, and controls the IOSNET, which enables inter-IOS communications. The HK68/V30 is present in each of the IOS configurations in the CRAY Y-MP EL system. The HK68/V30 located in IOS 0 is the system master (MIOP); any other HK68/V30s are slaves to the MIOP. For more detailed information on the composition and operation of the Heurikon HK68/V30, refer to the manufacturer's document HK68/V30/HK68/V30XE User's Manual.

Input/Output Buffer Board

The IOBB provides buffer memory for the IOP and acts as a communications interface between the IOS and the CPU. IOS-to-CPU communication takes place in the following manner: the IOP generates interrupts to initiate a CPU request, and the CPU generates interrupts to initiate a peripheral read or write operation or to terminate the CPU request. These interrupts are called I/O task control blocks (IOTCB), of which there are two types: I/O IOTCB and CONSOLE IOTCB. Both of these types have the same format with minor variations, as described in the following subsections.

I/O IOTCB Format

The format of an I/O IOTCB (S=0) is shown in Figure 4-1.

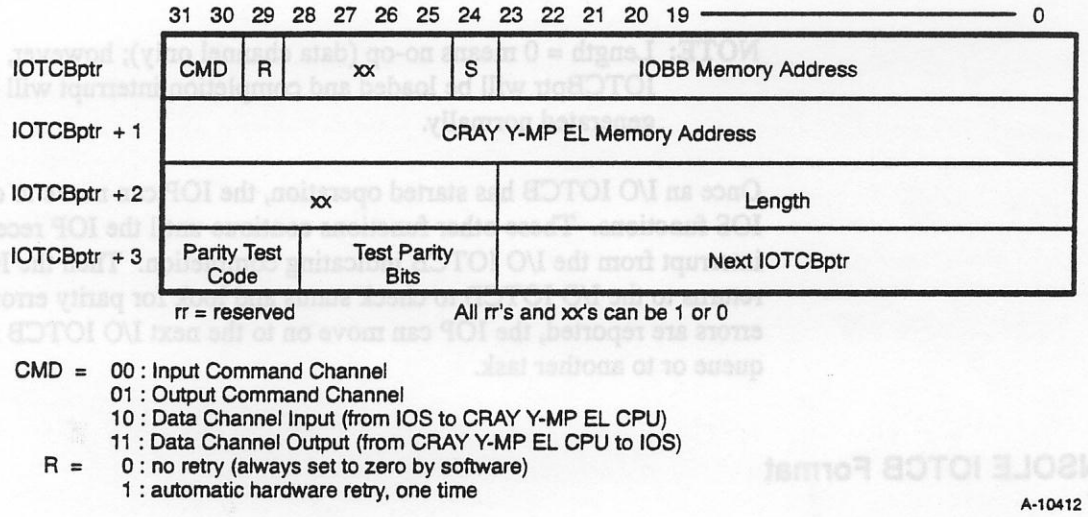


Figure 4-1. I/O IOTCB Format

IOBB Memory Address

IOBB memory address is the starting address in IOBB memory where data should be read from or written to. Twenty-two bits can address up to 4 million 32-bit words (16 Mbytes) of IOBB memory. The IOBB memory address is a 32-bit word address, and must be divisible by 32 (i.e., <4:0> = 00000) for a 32-, 64-, and 128-word burst.

CRAY Y-MP EL Memory Address

CRAY Y-MP EL memory address is the starting address where data should be read from or written to. This field is ignored by the CC if command (CMD) = 0x.

Length

Length is the number of 32-bit words to be transferred, limited by the total amount of memory on the IOBB. The length must be even (e.g., CC ignores bit 0). This field is ignored by the CC if CMD = 0x.

Next IOTCBptr

The IOBB memory address where the next IOTCB resides is the next IOTCBptr. The next IOTCBptr is a 32-bit word address, and must be divisible by 4 (i.e., <1:0> = 00).

NOTE: Length = 0 means no-op (data channel only); however, IOTCBptr will be loaded and completion interrupt will be generated normally.

Once an I/O IOTCB has started operation, the IOP can move to other IOS functions. These other functions continue until the IOP receives an interrupt from the I/O IOTCB indicating completion. Then the IOP returns to the I/O IOTCB to check status and look for parity errors. If no errors are reported, the IOP can move on to the next I/O IOTCB in the queue or to another task.

CONSOLE IOTCB Format

The format of a CONSOLE IOTCB (S=1) is shown in Figure 4-2.

When a CONSOLE IOTCB has started, the IOS waits for it to complete before moving on to another task.

Once a channel interrupt has been received, the IOP initiates an IOTCB, sends an IOTCB pending interrupt to the CC ASIC on the CPU, and waits for the CPU to acknowledge the interrupt. When the interrupt is received by the CPU, it is handled by the CC ASIC, which acts as the IOTCB processor within the CPU. The operating sequence for the channel operations is listed in the following subsections.

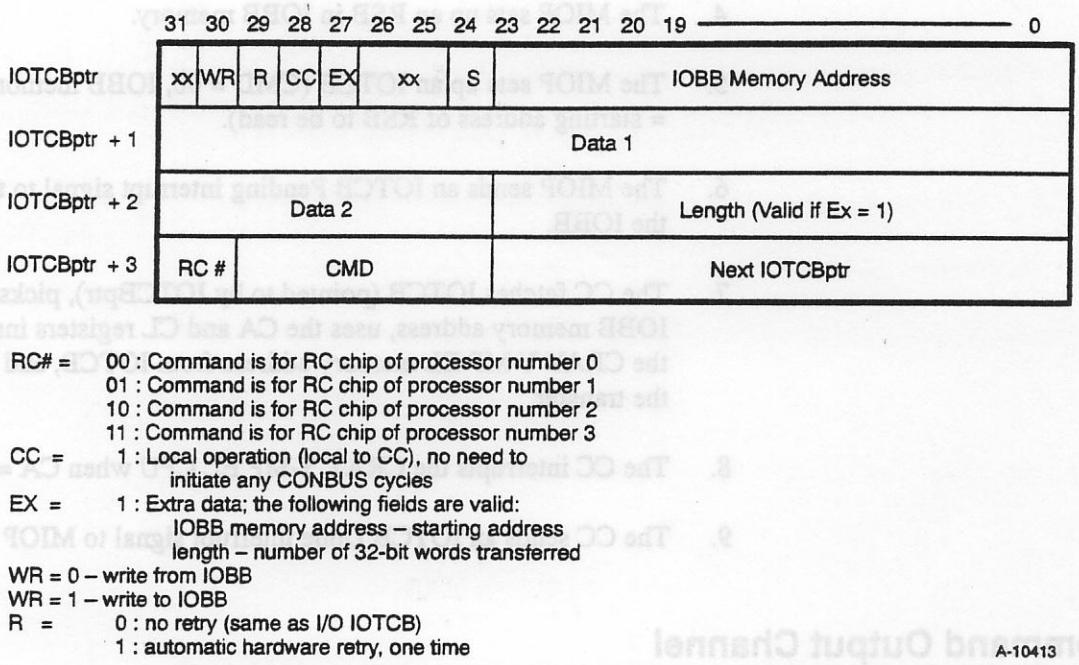


Figure 4-2. Console IOTCB Format

Command Input Channel

There are 5 registers in the CC associated with each input channel.

- Channel address (CA) -- the starting memory address in CRAY Y-MP EL memory
- Channel limit (CL) -- the ending memory address in CRAY Y-MP EL memory
- Channel error (CE) flag
- Channel interrupt (CI) flag
- Channel number (C#)

The operating sequence of an input channel is as follows:

1. The CPU loads the CL register.
2. The CPU loads the CA register; the corresponding input channel (C#) is opened.
3. The CC sends a Ready to Receive RSB interrupt signal to the MIOP via the IOBB.

4. The MIOP sets up an RSB in IOBB memory.
5. The MIOP sets up an IOTCB (CMD = 00, IOBB memory address = starting address of RSB to be read).
6. The MIOP sends an IOTCB Pending interrupt signal to the CC via the IOBB.
7. The CC fetches IOTCB (pointed to by IOTCBptr), picks up the IOBB memory address, uses the CA and CL registers instead of the CRAY Y-MP EL memory address from IOTCB, and completes the transfer.
8. The CC interrupts the CRAY Y-MP EL CPU when CA = CL.
9. The CC sends an IOTCB Done interrupt signal to MIOP via IOBB.

Command Output Channel

There are 5 registers in the CC associated with each output channel:

- Channel address (CA) -- the starting memory address in CRAY Y-MP EL memory
- Channel limit (CL) -- the ending memory address in CRAY Y-MP EL memory
- Channel error (CE) flag
- Channel interrupt (CI) flag
- Channel number (C#)

The operating sequence of an output channel is as follows:

1. The CPU sets up a control block (CB) in CRAY Y-MP EL memory.
2. The CPU loads the CL register.
3. The CPU loads the CA register; the corresponding output channel (C#) is opened.
4. The CC sends a CB Pending interrupt signal to the MIOP via the IOBB.
5. The MIOP sets up an IOTCB (CMD = 01, IOBB memory address = starting address for loading CB).

6. The MIOP sends an IOTCB Pending interrupt signal to the CC via the IOBB.

7. The CC fetches the IOTCB (pointed to by the IOTCBptr register), picks up the IOBB memory address, uses the CA and CL registers instead of the CRAY Y-MP EL memory address from IOTCB, and completes the transfer.

8. The CC interrupts the CPU when CA = CL.

9. The CC sends an IOTCB Done interrupt to the MIOP via the IOBB.

Data Channel (Input and Output)

The operating sequence of a data channel is as follows:

1. The MIOP sets up an IOTCB (CMD = 10 or 11).

2. The MIOP sends an IOTCB Pending interrupt signal to the CC via the IOBB.

3. The CC fetches the IOTCB (pointed to by the IOTCBptr register), interprets all parameters from the IOTCB, and completes the transfer.

4. The CC sends an IOTCB Done interrupt signal to the MIOP via the IOBB.

The IOBB also detects and reports errors. The Y1 bus enables parity transfers between the CPU and the IOBB. The IOBB can thus detect and report parity errors, of which there are two types: errors during IOTCB fetch and errors during IOTCB execution. If a parity error occurs during the IOTCB fetch operation, the CC ASIC is not allowed to complete the IOTCB. The CC will clear its IOTCB pending queue, reset the IOTCBptr register to zero, and send an IOTCB fetch error interrupt to the MIOP via the IOBB. To restart, the MIOP must load the next IOTCB to memory location zero on the IOBB, which is the default beginning of the IOTCB chain.

Errors that occur during IOTCB execution can also be of two types: command channel errors or data channel errors. In both cases, the execution of the IOTCB continues to completion, then the CC ASIC initiates a retry if the retry bit is set in the IOTCB. If this retry is not successful, an error message (IOTCB execution error) is returned to the MIOP. At this point, the operating system determines the procedure to follow for further error resolution.

Figure 4-3 shows how the IOBB fits into the communication path on the CRAY Y-MP EL system. Remember that the IOBB is a slave device to the IOP connected to it via the VMEbus. Refer to Figure 4-4 for a general block diagram of the IOBB.

Each of the Y1 buses has a channel pair number. Because the Y1 bus is bidirectional, it can be considered a channel pair. These channel assignments are as follows:

- CPU 0
  - CC0 - channels 20/21
  - ~~CC0 - channels 22/23~~
  - CC1 - channels 24/25
  - ~~CC1 - channels 26/27~~
- CPU 1
  - CC0 - channels 30/31 — 40/41
  - ~~CC0 - channels 32/33~~ — 42/43
  - CC1 - channels 34/35 — 44/45
  - ~~CC1 - channels 36/37~~ — 46/47
- CPU 2
  - CC0 - channels 40/41 — 60/61
  - ~~CC0 - channels 42/43~~ — 62/63
  - CC1 - channels 44/45 — 64/65
  - CC1 - channels 46/47 — 66/67
- CPU 3
  - CC0 - channels 50/51 — 100/101
  - ~~CC0 - channels 52/53~~ — 102/103
  - CC1 - channels 54/55 — 104/105
  - ~~CC1 - channels 56/57~~ — 106/107

Not Functional.

The Y1 bus channel pair associations apply to the channel number assignments of both the CRAY X-MP computer system and the CRAY Y-MP computer system. In this assignment scheme, the even-numbered channels are input channels, and the odd-numbered channels are output channels. The Y1 bus is bidirectional in the CRAY Y-MP EL system; therefore the association of channel numbers is for reference purposes only.

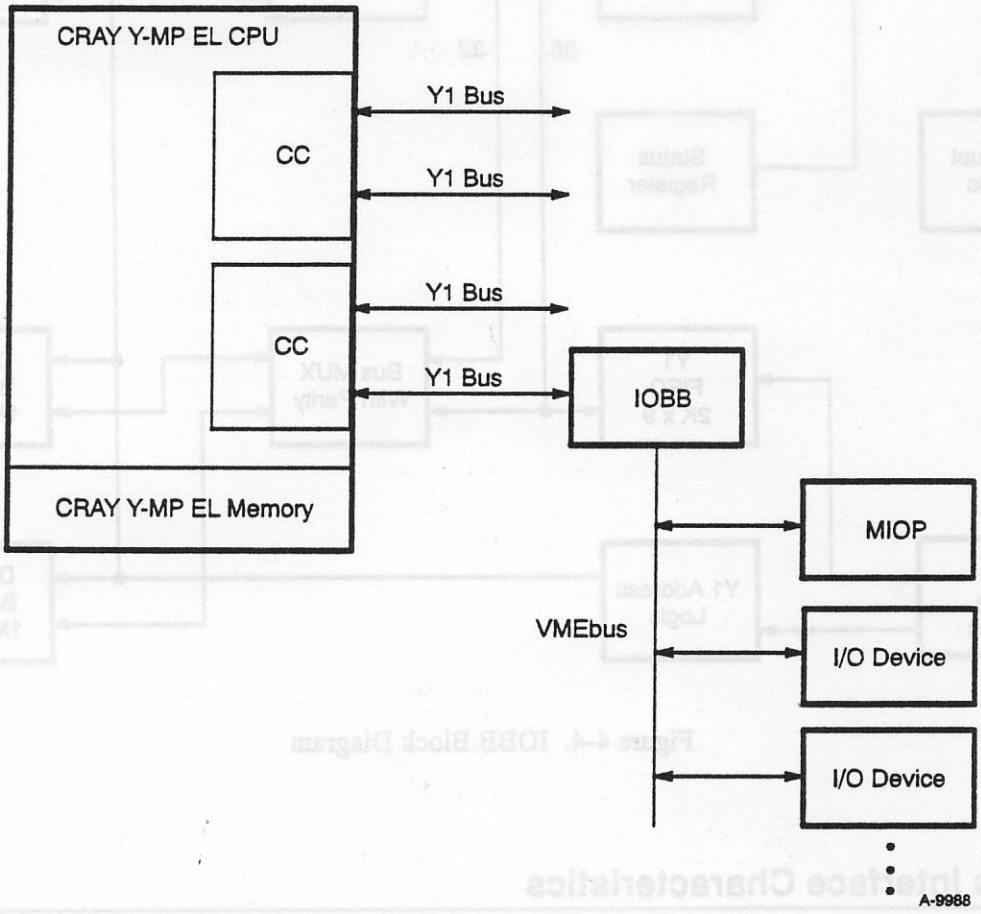


Figure 4-3. IOBB Communication

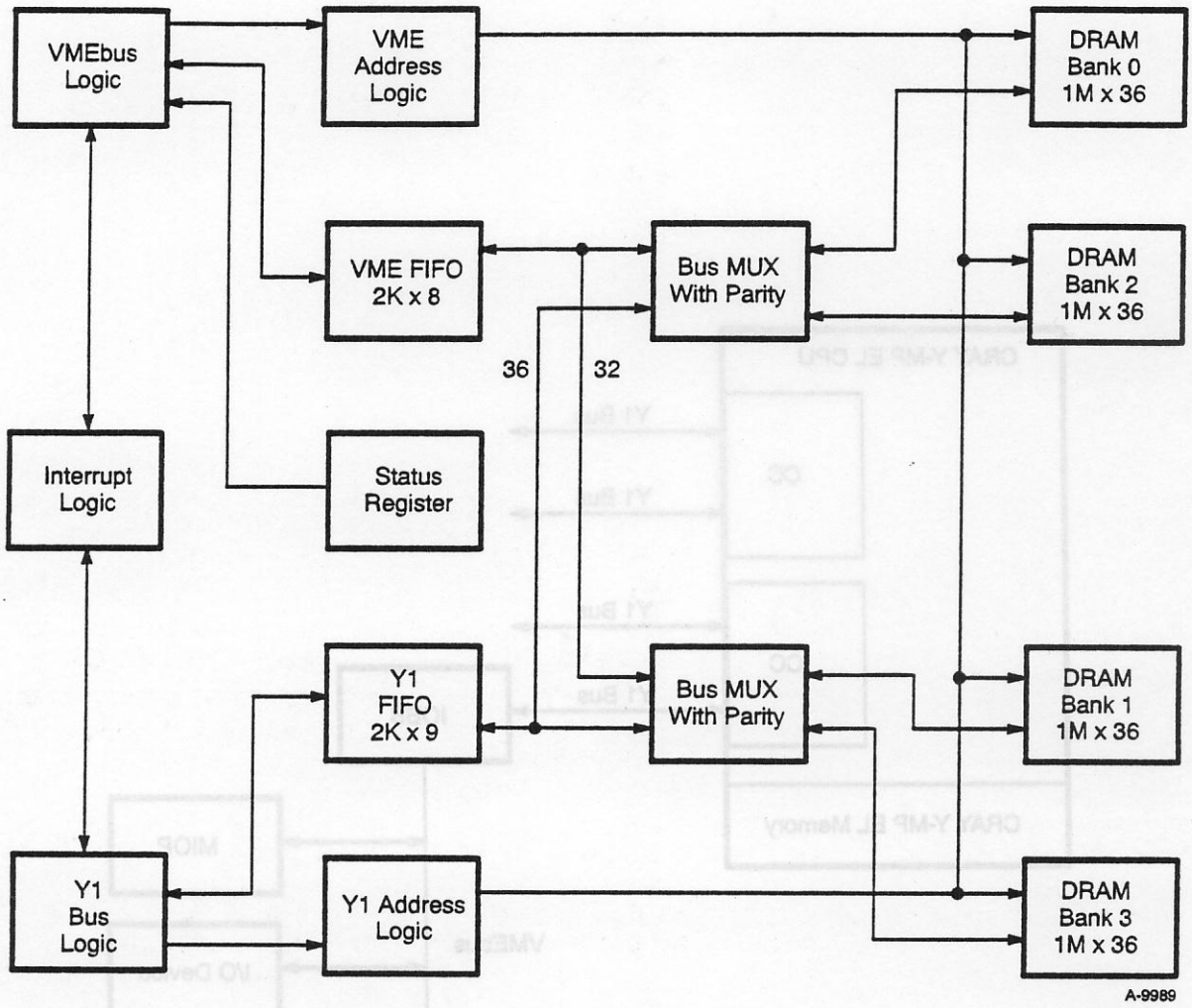


Figure 4-4. IOBB Block Diagram

VMEbus Interface Characteristics

All physical and electrical requirements conform to VMEbus Specification Rev D.

VME Slave Characteristics

- Maximum 80 Mbyte/s block-transfer rate (64-bit mode)
- Short (A16), standard (A24), extended (A32), and long (A64) addressing capabilities (for A64, only 32 address bits are used.)
- Address modifiers for data access only (no program access)

- Word (D16) or long-word (D32) data transfers
- Byte (D08 [O], D08 [E]) transfer in single cycle only
- No unaligned-transfer capability
- No read-modify-write capability
- Supports block transfers (D16, D32, and D64)

VME Interrupter Characteristics

Interrupts from the Y1 bus set appropriate bits of the status register. Any set bits of the status register cause an interrupt request of level 4 to the multiplex I/O processor (MIOP). An 8-bit vector, taken from the int_vector register (programmable from the MIOP) is placed on the VMEbus when the interrupt request is acknowledged, D08 (O). The MIOP should read the status register to find out the cause of the interrupt. When the IOBB detects a read of the status register, it resets the status register and releases the interrupt request, or RORA.

Control, Status, and Interrupt Vector Registers

There are two control registers, one status register, and one interrupt vector register on the IOBB. The control register performs the following functions:

- Short addressing (A16) from 1000 to 1003 with Jumper J1 absent
- Short addressing (A16) from 1040 to 1043 with Jumper J1 present
- Address modifier 29, 2D
- D16 transfers only

The status register contains 10 bits of information:

- Bit 9 set = Parity error detected on VME read from IOBB
- Bit 8 set = Received one or more Console Interrupt signals from the channel control ASIC (CC)
- Bit 7 set = Received one or more ready to receive Return Status Block (RSB) interrupt signals from CC

- Bit 6 set = Received one or more CB Pending interrupt signals from CC
- Bit 5 set = Received one or more Reset interrupt signals from CC
- Bit 4 set = Received one or more I/O task control block (IOTCB) Fetch Error interrupt signals from CC
- Bit 3 set = Received one or more IOTCB Execution Error interrupt signals from CC
- Bits 2 through 0 = The total number of IOTCB Done and IOTCB Execution Error interrupt signals received from CC; for example, 000 = none, 100 = 4.

The int_vector register contains the following information:

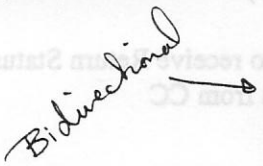
- Bit 15 set = Reset the I/O channel
- Bits 7 through 0 = The VME interrupt vector

All control information from the CC passes through the Y1 bus to the status register on the IOBB. However, there is no hardware interlock to ensure that the MIOP receives all the interrupts. For bits 7 through 5 of the status register, it is assumed that the CC will not send more than one interrupt of each type before the MIOP is able to read the status and respond.

If bit 4 of the status register is set, the MIOP should ignore bits 3 through 0, and restart by placing an IOTCB at IOBB memory location zero.

When bit 3 = 0, bits 2 through 0 indicate the number of IOTCBs completed successfully since the last time the status register was read. Because the maximum number of outstanding IOTCBs is 7, the MIOP must not start any more IOTCBs until completion interrupts are received by reading the status register. If bit 3 is set, one or more of the IOTCBs completed was not successful. The status register does not provide enough information to indicate which IOTCB was bad; therefore, the MIOP must retry the total number of IOTCBs indicated by bits 2 through 0.

Communications



The communications channel in the CRAY Y-MP EL system is called the Y1 bus. The Y1 bus is capable of 40-Mbyte/s transfer rates; these data transfers exist as data bursts of 4, 32, 64, or 128 thirty-two-bit words. The actual data signal is a differentiated value that provides a high level of noise immunity.

Y1 Bus Interface

The Y1 bus is a Cray Research, Inc. proprietary bus that connects the IOBB, located in the IOS, to the CC located in the CPU. The Y1 bus transfers data at high speed over long distances between the IOBB and the CC. The Y1 bus has the following characteristics:

- Point-to-point connection from the IOBB to memory; the IOBB is a slave memory
- The data bus is bidirectional, is 32 bits wide, and has byte parity
- Address, control, and data are time-multiplexed using the single 32-bit data bus
- Data bursts can be 4, 32, 64, or 128 thirty-two-bit words long
- Maximum burst rate is 80 Mbytes/s
- Maximum cable length is 50 ft
- Capable of passing interrupts in both directions at any time (independent of data transfers)
- All signals are differential for high noise immunity

Y1 Bus Signal Descriptions

Figure 4-5 shows the Y1 bus signals. The IOBB is in receive mode until conditioned by the CC bus signal. The subsections that follow describe each signal.

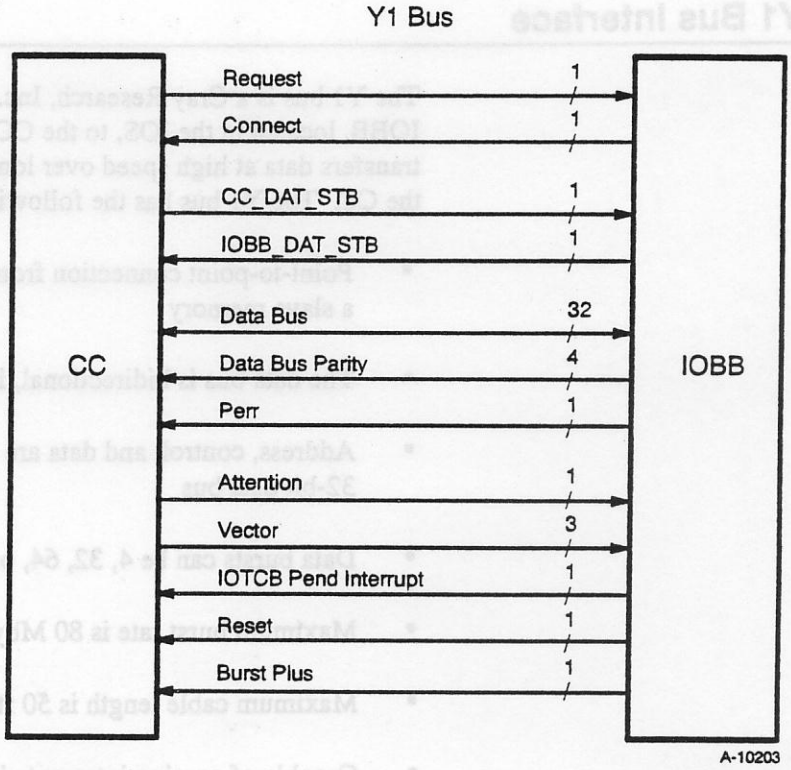


Figure 4-5. Y1 Bus Signal Descriptions

Request Signal (active high)

The CC communicates with the IOBB by placing the following information on the Data Bus signal. Refer to Table 4-1.

Table 4-1. Data Bus Information

Bits	Definition
<21:0>	IOBB memory address (addresses 4M 32-bit words)
<28:22>	Reserved (driven low)
<30:29>	00 = 32-word data burst
	01 = 64-word data burst
	10 = 128-word data burst
	11 = 4-word burst
<31>	1 = Data transfer from CC to IOBB (write)
	0 = Data transfer from IOBB to CC (read)

The CC then asserts the Request signal after this information has been valid on the Data Bus signal for a minimum of 50 ns. This information should remain valid on the Data Bus until the IOBB asserts the Connect signal. The IOBB can therefore use the rising edge of the Request signal to latch the information. The Request signal can be re-asserted only when the Connect signal has been negated. Each Request and Connect signal sequence can transfer a burst of 4, 32, 64, or 128 thirty-two-bit words of data.

Connect Signal (active high)

The IOBB responds to a Request signal by asserting the Connect signal to indicate that the address, direction, and burst size are latched. The CC should keep the address and direction on the bus until the Connect signal is asserted by the IOBB. The Request and Connect signals should remain asserted for the duration of the transfer, except on read operations where the CC may drop the Request signal after receiving a Connect signal from the IOBB. At the end of a write operation the CC should negate the Request signal. The IOBB responds by negating the Connect signal when it also detects the end of transfer.

CC_DAT_STB (active high)

CC_DAT_STB is used to send data from the CC to the IOBB. After connection is established by the Request and Connect signals (and the transfer is from CC to IOBB), 4, 32, 64, or 128 CC_DAT_STB pulses (bursts of data) should be sent to the IOBB. The maximum frequency of the CC_DAT_STB signal is one pulse every 50 ns, so the maximum burst transfer rate is 80 Mbytes/s. If the data transfer ends at a non-burst boundary, the last burst is less than 4, 32, 64, or 128 words.

Burst Plus Signal (active high)

When the Burst Plus signal is asserted, it informs the CC that the new IOBB is present so that faster burst transfer rates are possible and that burst lengths of 4, 32, 64, and 128 words are supported.

IOBB_DAT_STB Signal (active high)

The IOBB_DAT_STB signal is used to send data from the IOBB to the CC. After connection is established by the Request and Connect signals (and the transfer is from IOBB to CC), 4, 32, 64, or 128 IOBB_DAT_STB pulses should be sent to the CC. The maximum frequency of the IOBB_DAT_STB signal is one pulse every 50 ns, so the maximum burst-transfer rate is 80 Mbytes/s.

Data Bus and Data Bus Parity Signals (active high)

The Data Bus signal is a 32-bit bidirectional data bus with odd byte parity. The P3 signal is for bits 31 through 24, the P2 signal is for bits 23 through 16, the P1 signal is for bits 15 through 8, and the P0 signal is for bits 7 through 0. Data, address, direction, and burst length information is transferred via the Data Bus signal.

Perr Signal (active high)

The IOBB uses the Perr signal to report a parity error of address or data to the CC. The IOBB sends the Perr signal pulse whenever it detects a parity error during the data or address transfer sequence. The CC does not terminate the transfer when a parity error is detected. When address parity error is detected in the IOBB, the CC continues with the sequence of data transfers, but the IOBB does not write the data into its memory.

Attention and Vector Signals (active high)

The Attention signal is the interrupt signal from the CC to the IOBB. The three Vector signal bits indicate the reason for the interrupt. Refer to Table 4-2. These signal bits are only observed by using an oscilloscope.

Table 4-2. Attention and Vector Information

Vector <2>	Vector <1>	Vector <0>	Cause for the Interrupt
1	1	1	Console interrupt
1	1	0	CA is loaded to the input channel (ready to receive RSB)
1	0	1	CA is loaded to the output channel (CB pending)
1	0	0	Reset opcode is received in the output channel
0	1	1	IOTCB done
0	1	0	IOTCB fetch error
0	0	1	IOTCB execution error
0	0	0	Not used

The CC may send consecutive interrupts to the IOBB at a rate of one pulse (50 ns) every 330 ns. The IOBB saves the interrupts and vectors in the status register for the IOP to reference.

IOTCB Pend Interrupt Signal (active high)

The I/O task control block (IOTCB) is used by the IOP to request a data transfer between CRAY Y-MP EL system memory and the IOBB. When an IOTCB is ready in the IOBB memory, the IOBB interrupts the CC. The interrupt is a pulse 50 ns (minimum) wide. The CC can queue as many as seven IOTCB Pend Interrupt signal pulses without responding to them.

Reset Signal (active high)

The Reset signal resets the CRAY Y-MP EL channel to which the IOP is connected. This signal can be used to force the CC to search for the next IOTCB at location zero of the IOBB memory.

Y1 Bus Pin Assignments

The IOBB interfaces to the Y1 bus through two 60-pin connectors, P1 and P2, on the front panel of the board. Refer to Table 4-3 and Table 4-4.

Table 4-3. P1 Pin Assignments

P1 Pin	Signal Name	P1 Pin	Signal Name	P1 Pin	Signal Name
1	BURSTPLUS	21	GND	41	DB15P
2	GND	22	GND	42	DB15N
3	GND	23	DB08P	43	DB16P
4	GND	24	DB08N	44	DB16N
5	DB00P	25	DB09P	45	DB17P
6	DB00N	26	DB09N	46	DB17N
7	DB01P	27	DB10P	47	DB18P
8	DB01N	28	DB10N	48	DB18N
9	DB02P	29	DB11P	49	DB19P
10	DB02N	30	DB11N	50	DB19N
11	DB03P	31	Not Used	51	DB20P
12	DB03N	32	Not Used	52	DB20N
13	DB04P	33	DB12P	53	DB21P
14	DB04N	34	DB12N	54	DB21N
15	DB05P	35	DB13P	55	DB22P

Table 4-3. P1 Pin Assignments (continued)

P1 Pin	Signal Name	P1 Pin	Signal Name	P1 Pin	Signal Name
16	DB05N	36	DB13N	56	DB22N
17	DB06P	37	DB14P	57	GND
18	DB06N	38	DB14N	58	GND
19	DB07P	39	GND	59	GND
20	DB07N	40	GND	60	GND

Table 4-4. P2 Pin Assignments

P2 Pin	Signal Name	P2 Pin	Signal Name	P2 Pin	Signal Name
1	GND	21	GND	41	REQP
2	GND	22	GND	42	REQN
3	GND	23	DB31P	43	CONNP
4	GND	24	DB31N	44	CONNN
5	DB23P	25	DBP0P	45	TCBPENDP
6	DB23N	26	DBP0N	46	TCBPENDN
7	DB24P	27	DBP1P	47	PERRP
8	DB24N	28	DBP1N	48	PERRN
9	DB25P	29	DBP2P	49	VECT2P
10	DB25N	30	DBP2N	50	VECT2N
11	DB26P	31	RESET	51	VECT1P
12	DB26N	32	GND	52	VECT1N
13	DB27P	33	DBP3P	53	VECT0P
14	DB27N	34	DBP3N	54	VECT0N
15	DB28P	35	IOCCDRDYP	55	ATTNP
16	DB28N	36	IOCCDRDYN	56	ATTNN
17	DB29P	37	IOBBDRDYP	57	GND
18	DB29N	38	IOBBDRDYN	58	GND
19	DB30P	39	GND	59	GND
20	DB30N	40	GND	60	GND

Y1 Bus Channel Operations

The CRAY Y-MP EL system has two types of logical channels: command channels and data channels. CPU instructions control command input and command output channels. The CPU uses the output channels to send commands to the IOS and the input channels to receive status from the IOS. Data channels are controlled by the IOS. The IOS uses data channels to transfer data between CRAY Y-MP EL memory and IOBB memory.

All of the channel operations are initiated by the IOP in the form of IOTCBs. The IOP has to set up an IOTCB in IOBB memory for every transfer between CRAY Y-MP EL memory and IOBB (a maximum of 7 outstanding IOTCBs is allowed). There are two types of IOTCBs: an I/O IOTCB (S=0), and a CONSOLE IOTCB (S=1).

IOSNET

Communication between the IOP, the other IOSs, and the maintenance workstation (MWS) takes place via an RS-422 serial interface, called the IOSNET, that can sustain transfers of 1.2 Mbits/s. This is a serial interface; therefore, any point that is defective eliminates the string. Essentially, if the MIOP is down, the entire system is down.

Communications along the IOSNET are arbitrated by the MIOP. If IOP 4 needs to communicate with IOP 1, the actual communications path includes MIOP (IOP 4 – MIOP – IOP 1). Refer to Figure 4-6 for an illustration of this daisy chain. Figure 4-6 also shows the communication path from the MIOP to the required system peripherals via the SCSI interface. The required system peripherals are the 0.25-inch cartridge tape drive, the Winchester hard disk drive, and the helical-scan tape drive. The system console used with the CRAY Y-MP EL system is a WYSE model 60 using an RS-232 interface to the MIOP.

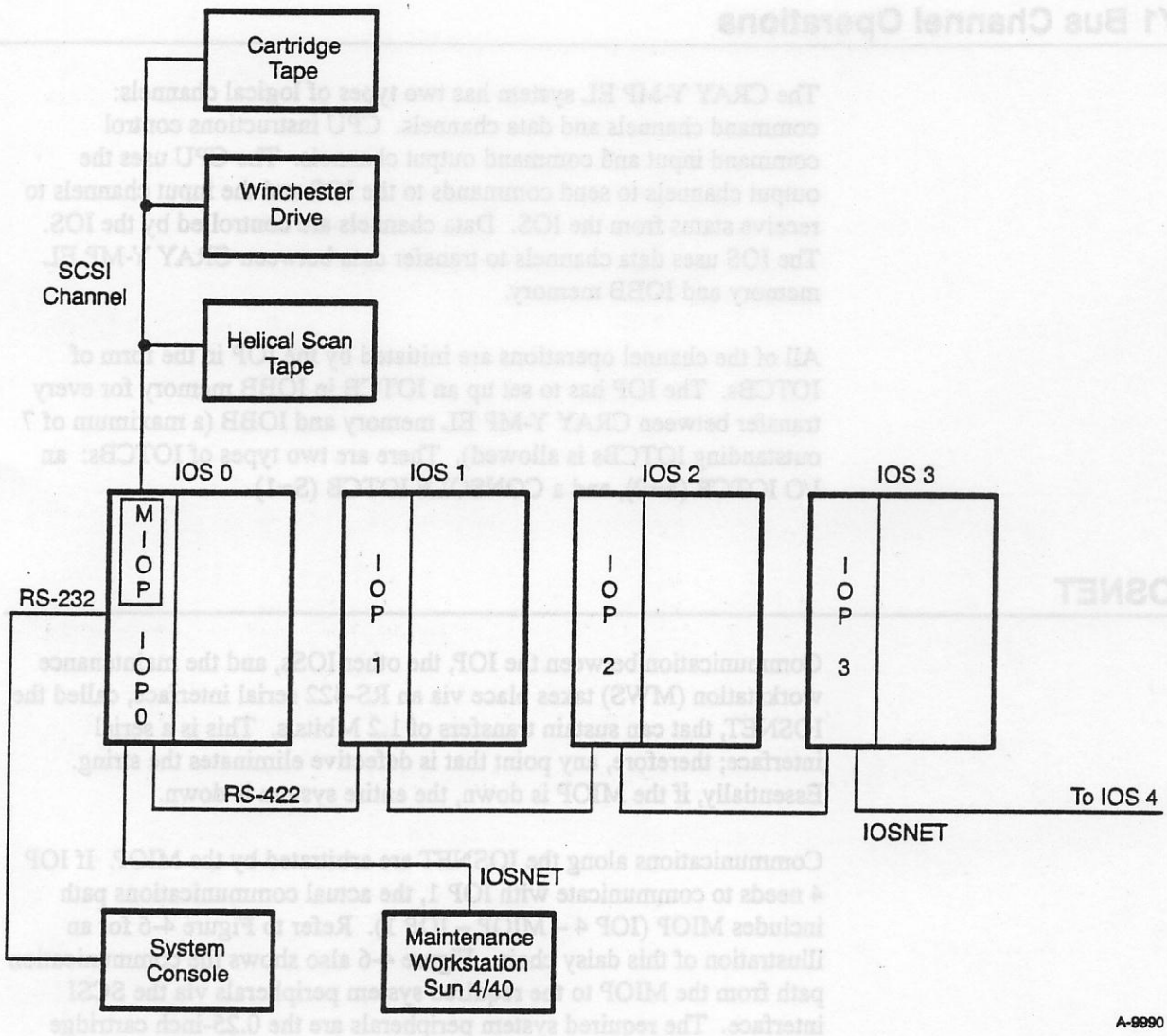


Figure 4-6. IOP Daisy Chain Configuration

IOS-supported Peripheral Controllers

The design of the IOS allows many different controllers to be installed. Consequently, many different peripheral devices can be connected to the CRAY Y-MP EL system. The minimum configuration that is available for the IOS includes a Heurikon HK68/V30 as the IOP, an IOBB, and one peripheral controller. Refer to Table 4-5 for the types of controllers supported by Cray Research, Inc.

Table 4-5. IOS-supported Peripheral Controllers

Device Type	Interface Protocol	Controller Vendor	Model Number	Peripheral Type	Cray Research Name
Tapes	SCSI	Heurikon†	HK68/V30	QIC 0.25 in. 9-track	MIOP
	SCSI	Heurikon†	HK68/V30	8-mm cartridge	MIOP
	Pertec	Ciprico Inc.	TM3000	9-track round tape	TC-2
	SCSI	Ciprico Inc.	RF3564	18-track cartridge (or) 8-mm cartridge (or) 18-track silo‡	SI-1
Disks	SCSI	Heurikon†	HK68/V30	3.5 in. Winchester	MIOP
	ESDI	Ciprico Inc.	RF3411	5.25 in. high density	DC-3
	IPI	Xylogics	SV7800	8 in. Sabre VII	DC-4
	ESDI array subsystem	Maximum Strategy	Bus master to a Strategy 2	5.25 in. ESDI array (10 disks per array)	DAS2
Network	Ethernet	CMC	130	Ethernet interface	EI-1
	FDDI	Interphase	4211	Fiber-optic channel	FI-1
	HYPERchannel	NSC	PI-492	HYPERchannel	HC-1

† The drive connected to the Heurikon SCSI channel in IOS 0 is a dedicated system device. The tapes on this channel are standard equipment and can be used by the customer.

‡ A customer may connect the CIPRICO SCSI controller to a Storage Technology Corporation 4781/4780 18-track cartridge silo transport. At present, these tape devices are not covered under Cray Research hardware maintenance.

Refer to Figure 4-7 for a configuration diagram of these devices. For a more complete description of the individual controllers, refer to the original equipment manufacturer (OEM) manuals supplied with the system.

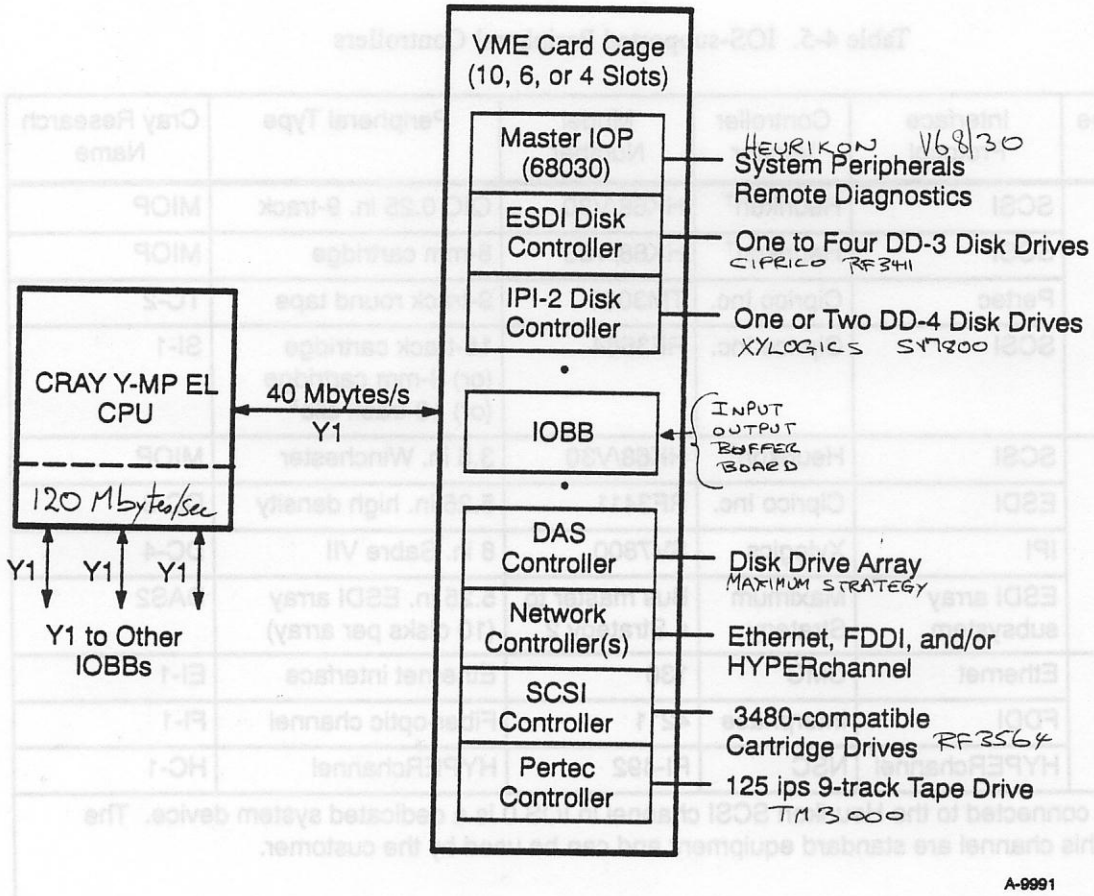


Figure 4-7. IOS Configuration

ALL Y1 SIGNALS ARE "ACTIVE HIGH"

5 PERIPHERAL DEVICES

The CRAY Y-MP EL computer system is designed with customer peripheral requirements in mind. The CRAY Y-MP EL system can accommodate a wide range of peripheral devices with a diverse amount of storage and communication capabilities. Because of this wide range of capabilities, in most cases it is best to refer to the original equipment manufacturer (OEM) manual for specific information on the equipment. Refer to Table 5-1 for a list of available peripheral devices and their characteristics.

Table 5-1. Peripheral Devices

Device Type	Manufacturer Model Number	Device Description	Storage Capacity	Transfer Rate (Peak)	Cray Research Name
Tapes	Archive Technology, Inc. Anaconda 2750	QIC 0.25-in. 9-track streaming cartridge †	1.6 Gbytes	600 Kbytes/s	N/A
	EXABYTE Model 8500	8-mm helical-scan EXABYTE cartridge †	5 Gbytes	4 Mbytes/s	EX-2
	Storage Tek Model 9914	0.5-in. 9-track TELEX 6–10.5 in. round tape	Encoding-dependent	6,250 bpi GCR mode	TD-2
	Storage Tek Model 4220	18-track cartridge (IBM 3480-compatible)	260 Mbytes	6,250 bpi GCR mode	TD-3
Disks	MDB Systems Data Cartridge	3.5-in. Winchester SCSI † ‡	204 Mbytes formatted	3 Mbytes/s	N/A
	MDB Systems Shuttle 500	3.5-in. removable SCSI ‡	204 Mbytes formatted	3 Mbytes/s	DR-2
	Hitachi DK516-15	5.25-in. ESDI drives in 8-drive PE-3 tray	1.32 Gbytes formatted	2.75 Mbytes/s	DD-3
	MDB Systems Data Shuttle 2100	5.25-in. removable ESDI with 2 drives per drawer ‡†	1.32 Gbytes formatted per drive	2.75 Mbytes/s per drive	DR-1

† The drive connected to the Heurikon SCSI controller in IOS 0 is a dedicated system device. The tapes on this channel are standard equipment and can be used by the customer.

‡ The actual disk incorporated by MDB is the Seagate Technology, Inc. ST1239 Swift.

‡† The actual disk incorporated is the Hitachi DK516-15 ESDI drive.

Device Type	Manufacturer Model Number	Device Description	Storage Capacity	Transfer Rate (Peak)	Cray Research Name
Disks (continued)	Seagate Technology, Inc. ST83050K	8-in. 2-hd parallel IPI in 2-drive PE-4 tray	2.7 Gbytes formatted	8.11 Mbytes/s	DD-4
	Hitachi DK516-15	5.25 in. ESDI array (10 disks per array) as controlled by the Maximum Strategy DAC	10.4 Gbytes per array	16 Mbytes/s per array	DAS-2

All of the peripheral devices are mounted in the cabinets available. The input/output subsystem (IOS) that controls the peripheral is normally included in the same cabinet. Figure 5-1 shows a typical layout of the various components within the system. The exact placement of any component is determined by the system configuration.

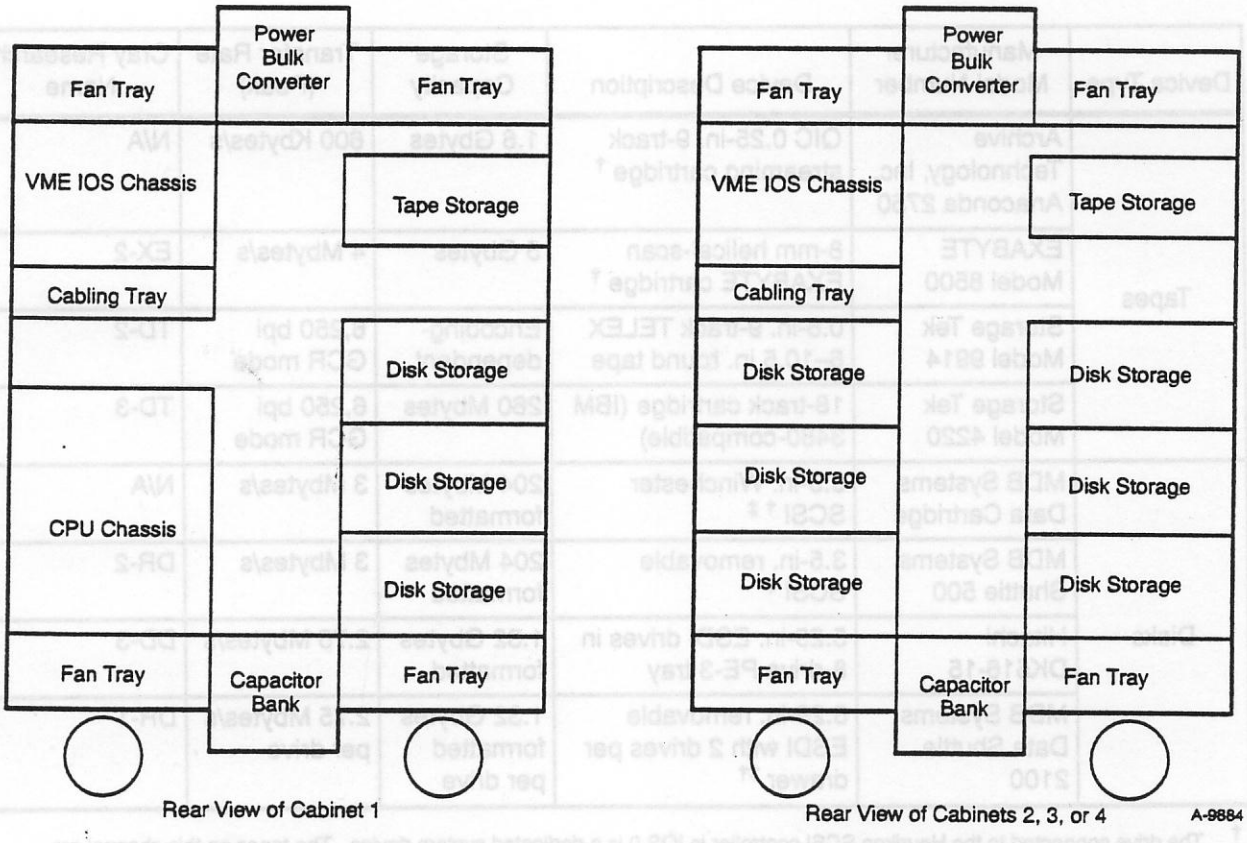


Figure 5-1. Example of Cabinet Layouts for the CRAY Y-MP EL System

The majority of the CRAY Y-MP EL system peripherals are field replaceable units (FRUs). This means that when one of the devices breaks down, it is completely replaced. There are no field-repairable parts inside the peripherals, except in the 9-track tape drive (TD-2), the 18-track tape drive (TD-3), and the disk array subsystem (DAS-2) controller. These components are described in the following subsections.

Flaw Management

For most disk drive subsystems, the main maintenance function of the product specialist will be disk media flaw management. Therefore, it is necessary to understand the naming conventions for the various disk drives in the CRAY Y-MP EL system. Refer to Figure 5-2.

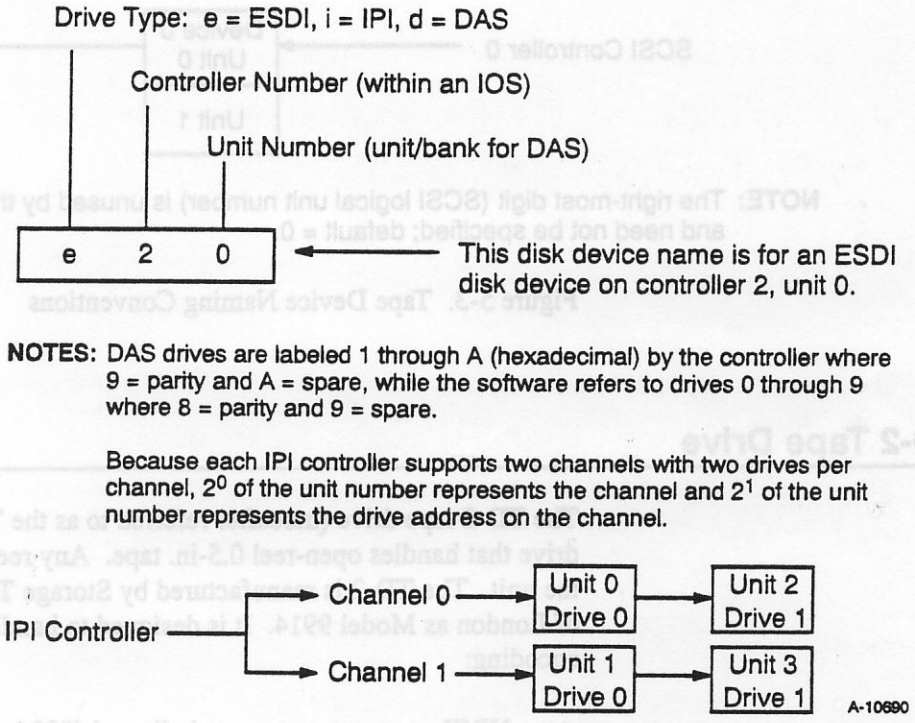
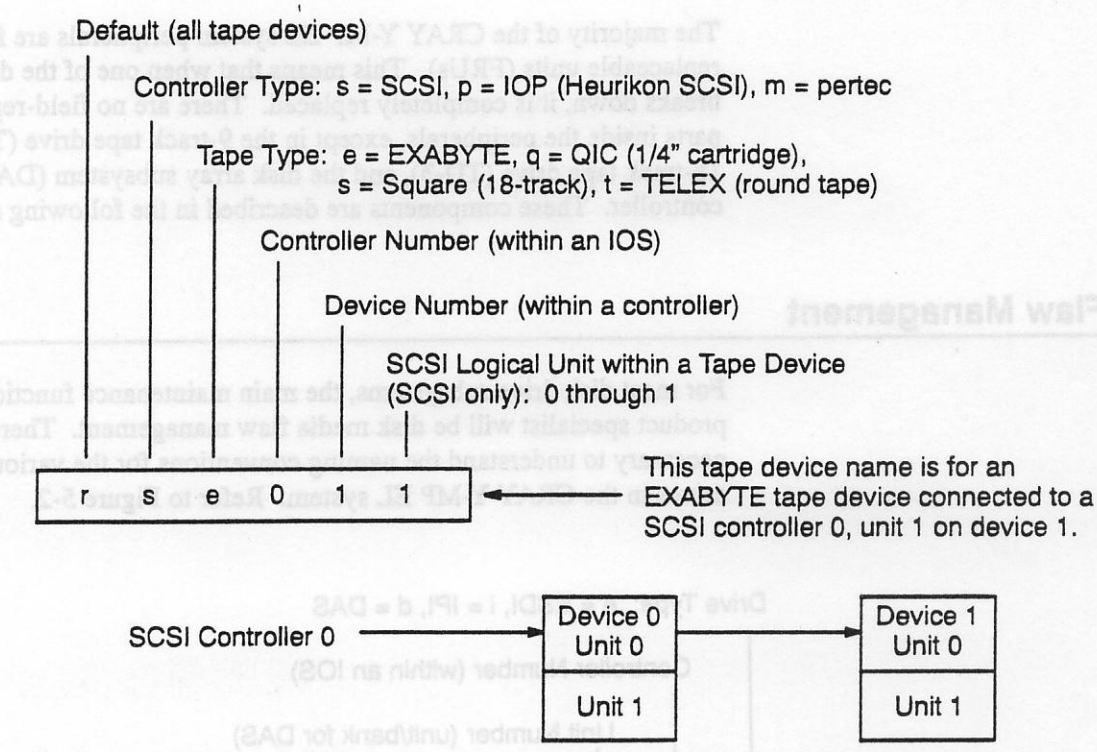


Figure 5-2. Disk Device Naming Conventions

Use the DFORMAT function or the DSLIP function described in the IOS Commands section of the CRAY Y-MP EL IOS Reference Manual for flaw management.

Although there is no flaw management with the system tape drives, they also conform to a set of naming conventions. The naming conventions for the tape drives in the CRAY Y-MP EL system are shown in Figure 5-3.



NOTE: The right-most digit (SCSI logical unit number) is unused by the other tape devices and need not be specified; default = 0.

A-10691

Figure 5-3. Tape Device Naming Conventions

TD-2 Tape Drive

The TD-2 tape drive (hereafter referred to as the TD-2) is a 9-track tape drive that handles open-reel 0.5-in. tape. Any reel up to 10.5 in. fits on the unit. The TD-2 is manufactured by Storage Tek Manufacturing, Ltd. of London as Model 9914. It is designed to handle four types of data encoding:

- NRZI - non-return to zero indicated (800 bpi)
- PE - phase encoded (1,600 bpi)
- DPE - double phase encoded (3,200 bpi)
- GCR - group coded recording (6,250 bpi)

The TD-2 is controlled by a pertec cache interface controller card, supplied by Ciprico Inc. as the TM3000 in the IOP. This pertec interface connects to another pertec cache contained in the TD-2, and is one of the FRUs of the TD-2. Other FRUs in the TD-2 are:

- Data control board (DCB)
- Digital data processor board (DDP)

- Analog data processor board (ADP)
- Servo control board (SCB)
- Power supply board (PSB) (contains two fuses)
- Hub sensor board (HSB)
- In-chute sensor board

Any other malfunctions that can occur are too complex for field repair, as they require an oscilloscope or other test equipment. In this case, removal and replacement of the entire TD-2 is required.

TD-2 Operator Functions

The customer operator can perform the following tasks by using the switches located at the front of the TD-2:

- Switch power ON or OFF.
- Select the recording density, which determines the data encoding.
- Place the TD-2 online. The UNICOS operating system controls the TD-2 when it is online.
- Place the TD-2 in offline mode.
- Rewind the tape to beginning of tape (BOT).
- Unload the tape.

Refer to Figure 5-4 for a diagram of the front (operator's) panel. The shaded areas of the panel indicate membrane-type switches; the other items represent lighted displays. The area showing the legend OFFLINE is a liquid-crystal display capable of displaying a large variety of messages. The other displays shown are back-lighted, single message displays that are illuminated when the particular condition exists in the TD-2. For a more detailed explanation of these controls and displays, refer to the manufacturer's manual for the TD-2.

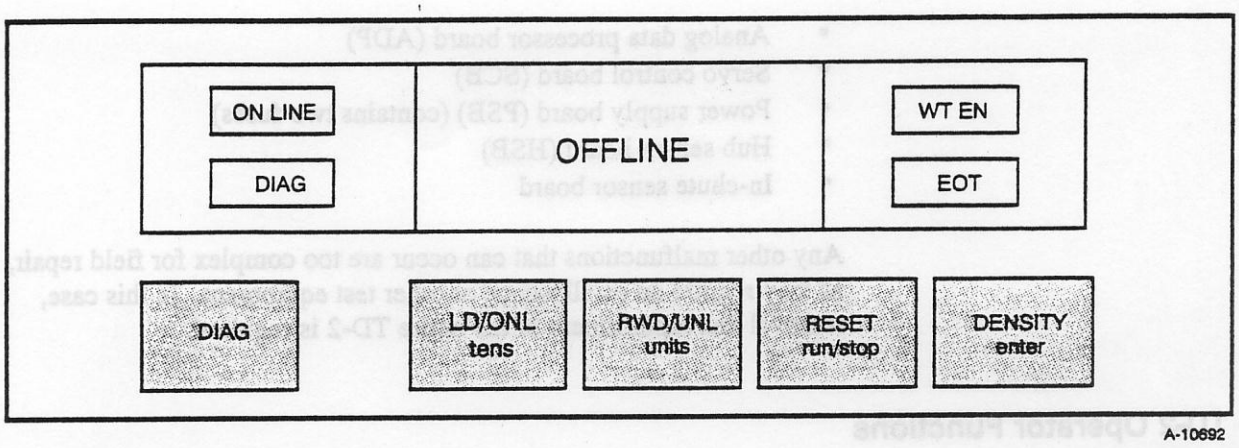


Figure 5-4. Operator Panel

When power is applied to the TD-2, a set of internal diagnostics is run. These diagnostics are referred to as power-on/reset (POR) diagnostics and reside in non-volatile random access memory (NVRAM). While these diagnostics are running, the liquid-crystal display (operators display) displays the message TESTING. When the POR diagnostics successfully complete, the operator is prompted to load a tape into the tape loading chamber and begin operation.

If there is a malfunction of the POR diagnostics, the operator display shows a fault message. The messages that may be displayed are shown in Table 5-2, along with a possible cause for the failure.

Table 5-2. POR Messages

Message	Possible Cause
Blank display	Main power is not available, the +5-volt supply is not operating, or the servo control bus is faulty.
CON VAL x	Usually a missing or disconnected subassembly (x is a number from 1 through 7).
OK	The POR checks have completed successfully.
POWER	A fault has been found with the power supply board while all the internal power supply lines were being checked for normal limits.
TESTING	Power-up message indicating the POR checks are in progress.

The procedure that occurs when power is applied to the TD-2 is:

1. The operator panel indicates TESTING. This means the POR diagnostics are running.
2. The operator panel momentarily indicates OK. This means the POR diagnostics have successfully completed.
3. The operator panel displays LOCATING. While this display is illuminated, the supply hub is rotating back and forth for several seconds.
4. The operator display indicates NO TAPE. This indicates completion of the POR sequence, and prompts the operator to begin normal operation.

To load a tape at this time, the operator is prompted to press the RESET on the operator panel. It is important to note that the tape loading door cannot be opened manually; there is not a manual latch release mechanism. The only way that the loading door can be opened is by releasing the solenoid that locks the door during operation. If it becomes necessary to manually open the tape loading door as a fault/maintenance procedure, it is necessary to extend the TD-2 from the mainframe chassis. Once extended, the tape path cover must be opened by releasing the three latches holding the tape path cover closed. Then, using a pointed instrument, it is possible to manually push the closing latch away from its locked position, thus opening the tape loading door.

Once the tape loading door is opened, it is possible to either load or unload a tape. The TD-2 is capable of containing tapes from a 6-in. diameter to a 10.5-in. diameter. To unload a tape, simply grasp the tape and remove it. To load a tape, place the tape into the tape chamber and close the tape loading door. At this time, the TD-2 takes over the load operation.

The TD-2 first causes the supply hub to rotate back and forth, moving the tape reel into position over the hub. Once in position, the hub locks the reel into place, turns on the vacuum motor, and begins rotating in a counter-clockwise (rewind) direction. Thus, the tape is loosened on the reel, pulled into the tape chute by the vacuum, then rewound by the supply reel. This action can occur two or three times, and ensures that the tape reel is inserted right side up, which is determined by an optical sensor 'seeing' the tape (being pulled by the vacuum), then not 'seeing' the tape (being rewound). The result of this action is that the supply motor reverses and starts unwinding tape. The tape is pulled through the tape path by the vacuum and wraps itself around the take-up reel. Once the take-up reel has secured the tape, the tape transport mechanism takes over and performs several functions.

If the load operation begins to unwind tape during the initial sensing cycle (that is, if the optical sensor does not see, then not see, the tape), the TD-2 determines that the tape reel is inverted. In this case, the operator display will display the message REEL INV, the supply hub motor rewinds the tape by doing a fast-forward operation, the supply hub unlocks the reel, and the operator begins indicating that RESET must be pushed to remove and invert the reel.

When the tape load operation is completed correctly, the TD-2 will 'shoe-shine' a small portion of tape. During this operation, the hardware is doing a read operation on actual data written on the tape. Then, firmware compares the written data with imbedded samples and determines the density that was used to write the tape. During the comparison period, the operator display contains the message ANALYZE. When analysis is finished, the display shows the density and the firmware sets to decode that tape. The TD-2 now begins a period of mechanical motion, searching forward and backward, until it locates beginning of tape (BOT). When this operation completes, the message BOT is displayed, alternating with density. This completes the load sequence. During this sequence, several messages are displayed. If the sequence fails, several other messages can be displayed. These messages are detailed in Table 5-3.

Table 5-3. Operator Display Messages

Message	Indication
ANALYZE	The tape has reached BOT and the data circuits are reading the ident burst to determine its recorded density. '
BOT	Tape is at BOT and loading is complete. When set online, the display changes to 'LD POINT' and the TD-2 is able to respond to host commands.
DOOR	The loading door (or the tape path cover) is open after a loading sequence started.
HUB LOCK	Shortly after loading has been initiated, the reel has been clamped onto the supply hub.
HUB ERR	Incorrect seating of the supply reel on the supply hub.
IN LIMIT	The tension arm has reached the limit if its travel and tape tension has been lost.
LID OPEN	Loading has been initiated, but the tape path cover turnbuckles are not secured.
LRG REEL	Near the end of the loading sequence, the firmware has detected that a large (10.5-in.) reel has been used.
LOADING	The reel has been clamped and the tape is being threaded along the tape path. **NOTE:** If LD/ONL is pressed during loading, the ONLINE legend illuminates immediately; at BOT, the TD-2 will be under the control of the host.

Table 5-3. Operator Display Messages (continued)

Message	Indication
LOCATING	Immediately after loading has been initiated, the reel is being maneuvered so as to lie flat on the supply hub, prior to clamping.
LOCKING	After loading has been initiated, the reel is clamped onto the supply hub.
MED REEL	Near the end of the loading sequence, the firmware has detected that a medium (8.5-in.) reel is being used.
NIC	Not in chute. During the early stages of loading, tape was not detected in the tape path chute.
NO TAPE	After loading has been initiated, the reel locating process concludes that no tape is present on the supply hub.
NTU	No take-up. During the later stages of loading, tape was not gripped onto the take-up reel.
OK	The POR checks were successfully completed.
REEL INV	During the early stages of loading, the tape reel was found to be inserted with the write protect ring up.
RESET	During the loading sequence, the RESET button was sensed as permanently depressed. Engineering assistance is required.
**TAB	The BOT tab was not detected near the end of the loading sequence. This tab must be present, within ANSI/ECMA specifications from the physical end of the tape.
REWIND	The tape is rewinding following either host or operator rewind command. This sequence completes at BOT. If RESET is pressed during rewinding, tape motion stops and the REWIND indication is replaced by 'Offline'.
REW/UNLD	An operator rewind and unload command has been given by holding RESET depressed and depressing RWD/UNL button.
SML REEL	Near the end of the loading sequence, the firmware has detected that a small (6- or 7-in.) reel is being used.
TAPE NOT IN CHUTE	Scrolled message: the tape end has not entered the tape path.
UNLOAD	An unload sequence is in progress following the pressing of the RWD/UNL button with BOT indicated. When the unload sequence is complete, the display changes to READY.
UNLOCK	The reel is being unclamped. NOTE: UNLOAD followed by UNLOCK could be the result of failing to detect the BOT marker.

At the product specialist level, there are no preventative maintenance measures required. However, periodic maintenance is required by the operator. This maintenance consists primarily of cleaning the various components in the tape path. It is possible for operator maintenance to cause or reveal a fault condition. Because of this, it is good practice to be aware of the required maintenance procedures, which can be found in the OEM manuals available with the CRAY Y-MP EL system.

TD-2 Field Replaceable Units

As mentioned earlier, there are several FRUs contained in the TD-2. Failures on any of these FRUs can be located by using the onboard diagnostics. These diagnostics are run by using the front panel switches on the TD-2. Other than a tape device that indicates failure, there are no provisions for maintaining the TD-2 via remote diagnostics. Faults must be isolated on site.

For complete information on how to run and interpret these diagnostics, refer to the Storage Tek user/diagnostic manual (# 95121796). Because several combinations of front panels, switches, and diagnostic programs are available, Storage Tek service and diagnostic manuals must be used as references.

When the failure is diagnosed to the FRU level, the FRU must be replaced using the procedures provided in the Storage Tek servicing manual (# 95121797). It should be noted that there are no individual tape-path FRUs. Instead, the entire tape path subassembly is removed in case of failure. When you remove or insert the tape path subassembly, ensure that the Tacho roller is not misaligned on its pivot shaft. The Tacho roller and the heads are the only components that can be damaged, and can cause the TD-2 to malfunction.

The read/write heads can also be damaged during normal removal and replacement. These heads are thin film heads and are useless if they are scratched. As a precaution when you remove or install the tape path subassembly, cover the heads with an adhesive bandage. Place the cloth pad over the face of the heads and press the adhesive to the sides. Ensure that the adhesive does not contact the face of the heads. After you install the tape path subassembly, clean the heads to ensure proper operation.

TD-3 Tape Drive

The TD-3 tape drive (TD-3) is also supplied by Storage Tek as the Model 4220 cartridge tape subsystem. The TD-3 is an 18-track tape drive that is IBM 3480-compatible.

The TD-3 comprises several subsystems. These subsystems include:

- Tape transport
- Servo electronics
- Disk drive electronics
- Read/write electronics
- Pneumatics
- Operator control panel
- DC power supply

The disk drive subsystem provides the TD-3 with both functional and diagnostic microcode. The floppy disk drive uses a 3.5-in., 720-Kbyte format, and is controlled by a single integrated circuit mounted on the system board (SB). Generated signals are sent to or from the drive through the bottom card (BT). The BT contains only foil runners (no active components); therefore, if there is a failure involving the floppy drive, the failing FRU is probably the drive itself or the SB.

As is true in any electro-mechanical device, three types of failure can occur in the TD-3: power-level electrical, mechanical, and signal-level electronic.

Power circuitry for the TD-3 is designed to accommodate either 100 to 120 Vac or 200 to 240 Vac, switch selectable from 47 to 63 Hz, single phase. From this input, the TD-3 supplies + 5 Vdc, +/- 12 Vdc, and + 24 Vdc to the various subassemblies. The only location in the TD-3 where AC power voltages exist is at the DC power supply board (DCPS). All voltages internal to the TD-3 are DC voltages. Refer to Figure 5-5 to locate the power supply.

The mechanical processes of the TD-3 are contained primarily on the tape deck. These mechanical processes deal with loading, unloading, and moving the tape after the cartridge is inserted into the deck. Figure 5-6 and Figure 5-7 show the location of the mechanical FRUs. When a mechanical problem occurs, the problem could be caused by another nonmechanical subassembly. For instance, the servo circuitry could be providing values to the mechanical assemblies that emulate a mechanical problem.

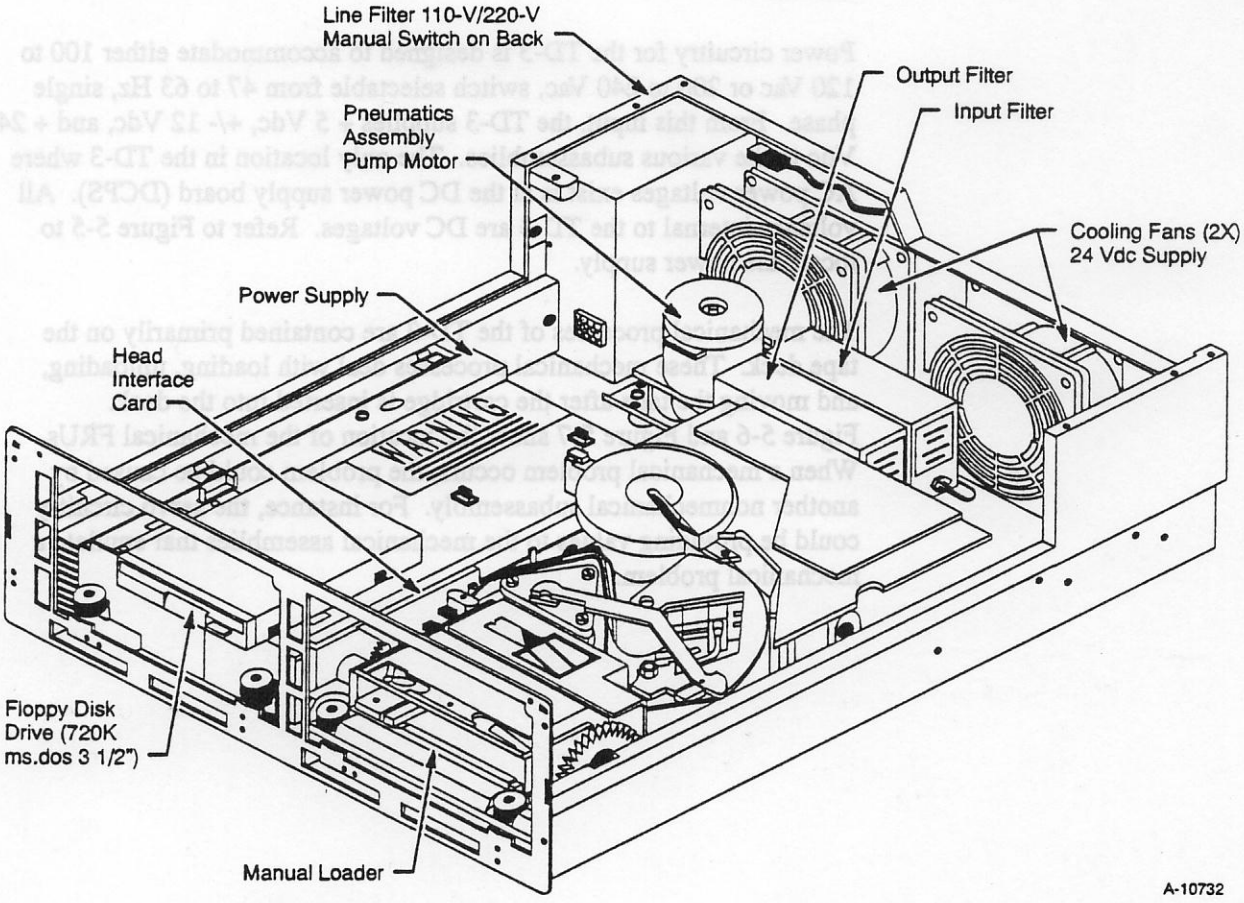


Figure 5-5. TD-3 Tape Drive (Power Supply)

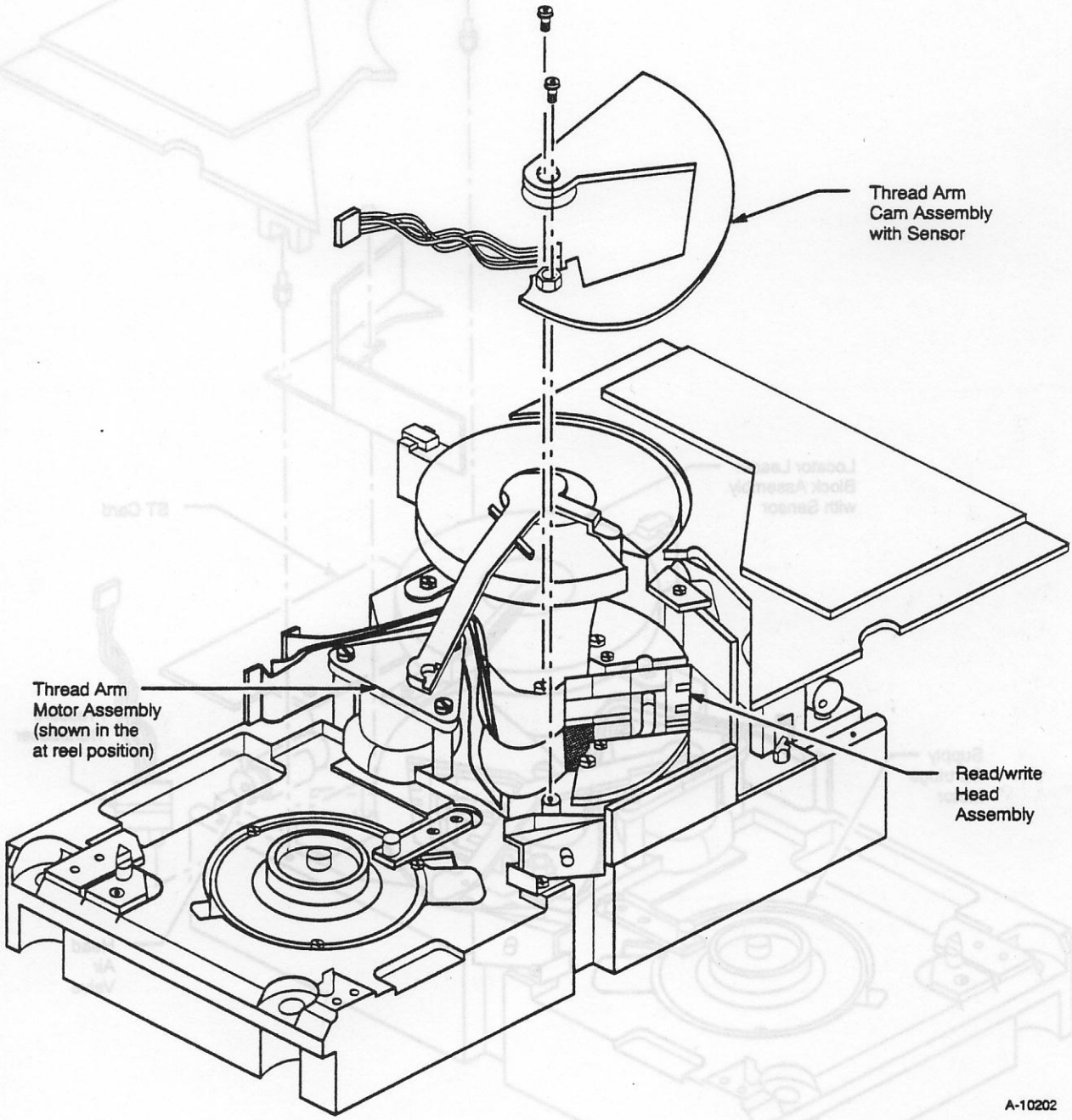


Figure 5-6. TD-3 Tape Drive (FRUs)

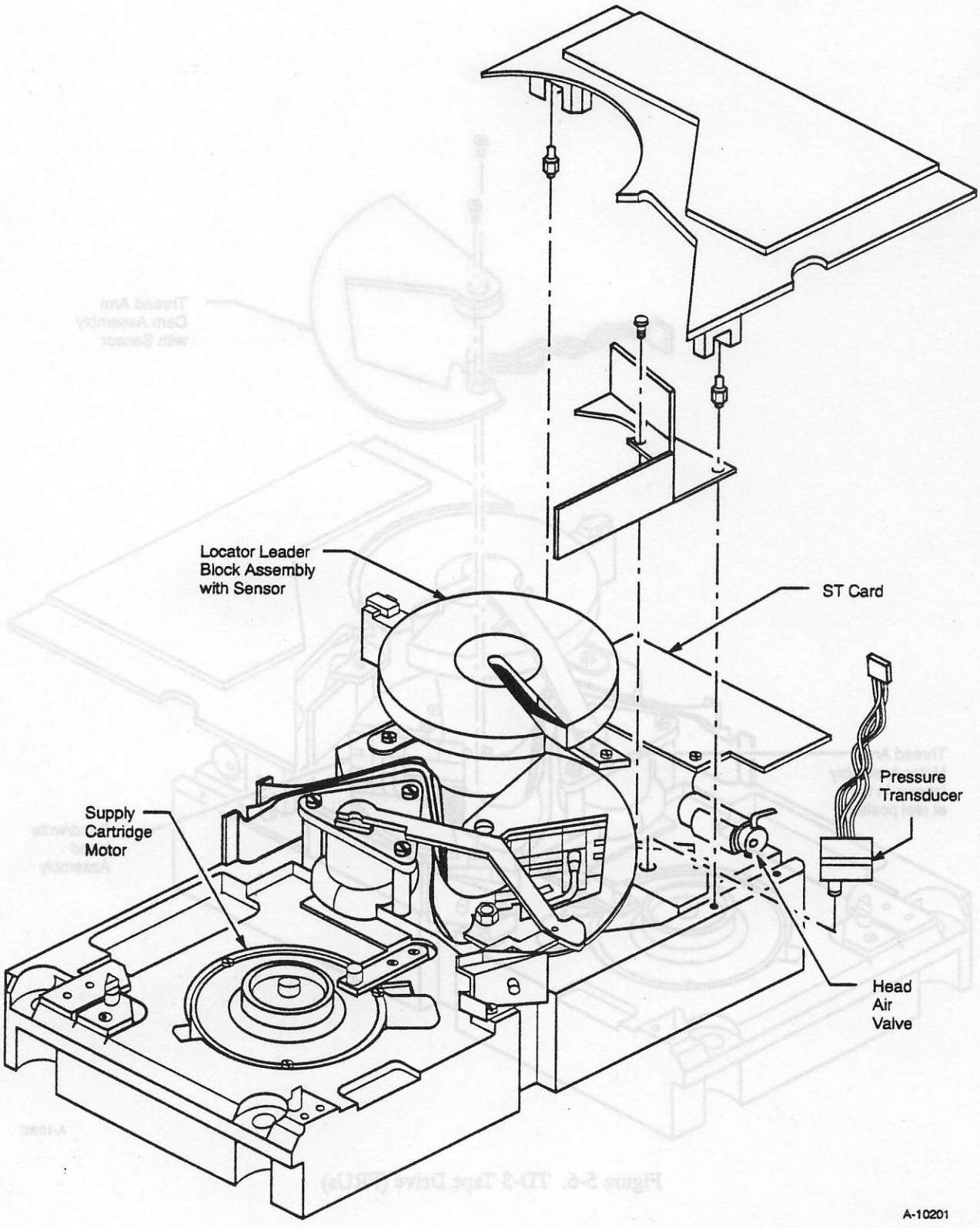


Figure 5-7. TD-3 Tape Drive

Diagnostic Functions

The TD-3 cannot be diagnosed from a remote location. A failing FRU within the TD-3 must be identified by using the front panel to load, run, and read the diagnostics and the error codes associated with them. Figure 5-8 shows the front panel of the TD-3. Note that there are four buttons on the panel, two of which are important to loading and running diagnostics: the scroll and the select buttons.

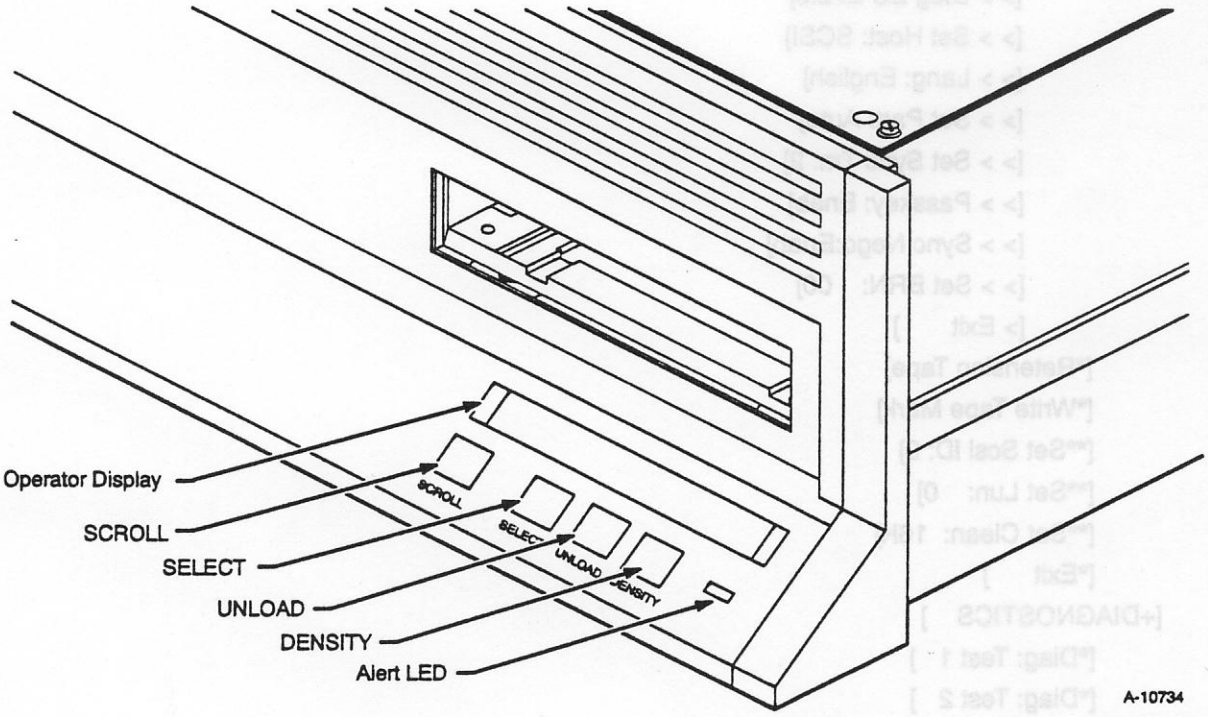


Figure 5-8. TD-3 Tape Drive Front Panel

The scroll button advances the display through a menu, one step at a time. The menu is shown in Figure 5-9. When you reach the desired location in the menu, use the select button to select (lock in) the item. Then, push the select button a second time to run the selected item.

For a complete list and a more detailed explanation of the individual diagnostics available for the TD-3, refer to the Storage Tek manual for the Model 4220 that is supplied with the system. That manual contains an extensive explanation of the diagnostics, the error codes as returned to the operator display, and a complete FRU guide.

Offline Menus

```
[OF:DIAG:       *]
[+SUBSYS STATUS]
     [*Online Request]
     [*Exit     ]
[+SET OR DISPLAY]
     [**CONFIGURATION]
          [> > Set Diags:None]
          [> > Diag EC LVL:0]
          [> > Set Host: SCSI]
          [> > Lang: English]
          [> > Set Part: Auto]
          [> > Set Sync Tm: 2]
          [> > Passkey: Enab]
          [> > Sync Nego:Enab]
          [> > Set BRN:   00]
          [> Exit      ]
     [*Retension Tape]
     [*Write Tape Mark]
     [**Set Scsi ID: 0]
     [**Set Lun:   0]
     [**Set Clean:  16K]
     [*Exit     ]
[+DIAGNOSTICS   ]
     [*Diag: Test 1   ]
     [*Diag: Test 2   ]
     [*Diag: Test 3   ]
     [*Diag: Test 4   ]
     [*Diag:Load/Unld]
     [**Diag: Loop 1]
     [Diag: Test Disp]
     [*Loader Sensors]
     [*Disply Pressure]
     [*Disply Tension]
     [*Exit     ]
[+SAVE TRACE   ]
     [*Save Trc: All]
     [*Exit     ]
```

Online Menus

```
[          *]
[ON:IDLE:     *]
[+SUBSYS STATUS]
     [*Offline Request]
     [*Exit     ]
```

Figure 5-9. Basic 4280 Menus with a SCSI Interface

Electrical Information

The following printed circuit (PC) boards comprise the signal-level electronics portion of the TD-3. Figure 5-10, Figure 5-11, and Figure 5-12 show the locations of these PC boards.

- Capacitor (CP) card
- Servo motion (SM) card
- Servo power (SP) card
- Read interface (RI) card
- System (SB) card
- Head interface (HI) card

Note that the PC boards reside on or under a tip-up lid on the top of the TD-3 (except the SCSI board) and cannot be accessed unless the TD-3 is extended from the rack. Follow the procedure provided in the FRU section of this manual to extend the TD-3.

The RI card controls generation of clock pulses for each track of data via three phase-locked loop (PLL) oscillators. The RI board also contains the write data encoders and peak detectors.

The SB card is the heart of the TD-3. It contains a 68010 microprocessor that processes host commands, provides I/O interface control, and controls the physical processes relating to tape operations. The SB card also includes a write formatter (WF) IC, a 2-Mbyte buffer, buffer FIFOs, an 8031 bus processor, deskew buffers, a floppy disk controller, and read data formatter devices. Be aware that all operations in the TD-3 are linked to the SB. When you troubleshoot the TD-3, remember that the SB may be faulty.

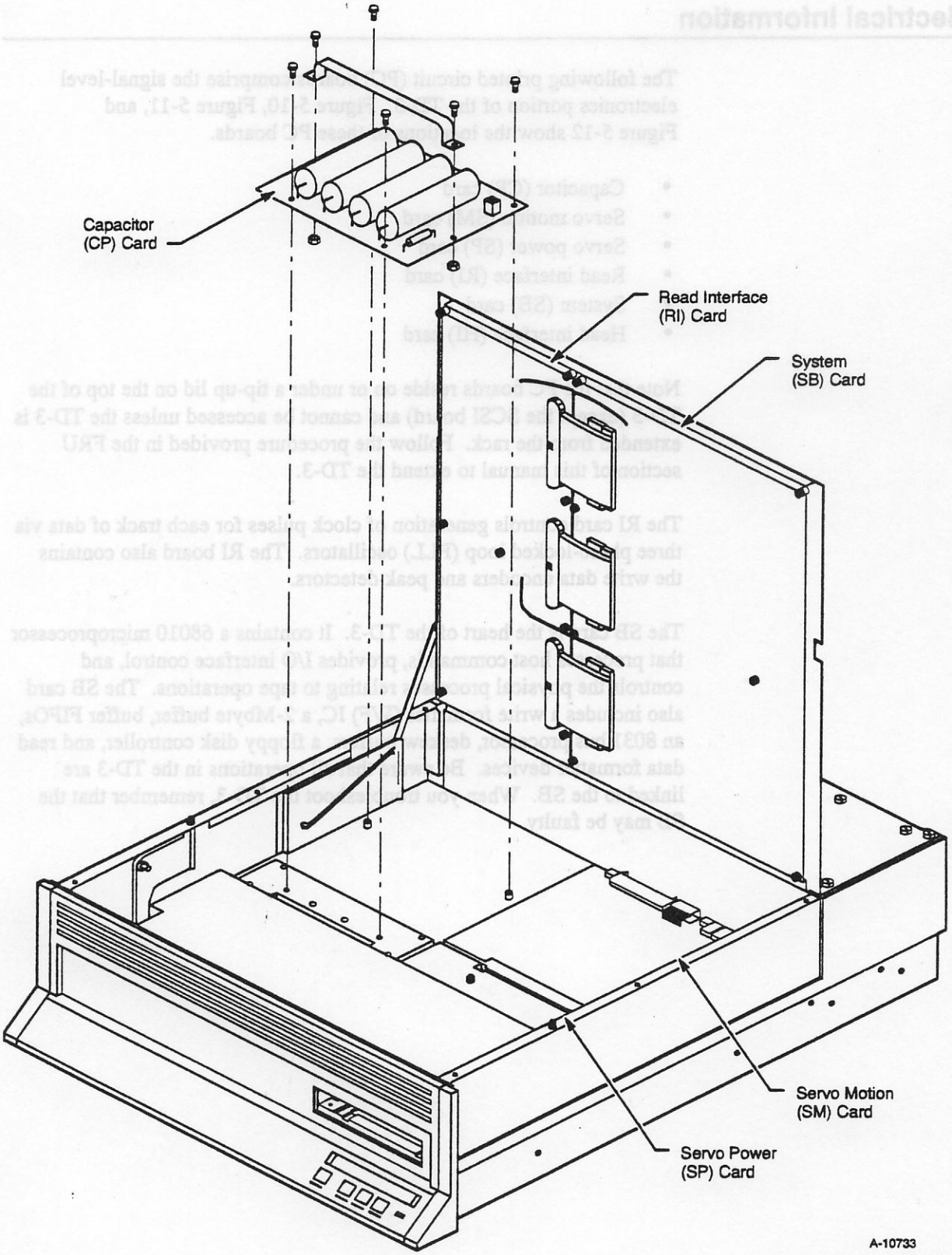


Figure 5-10. TD-3 Tape Drive Controller Module FRUs (Front View)

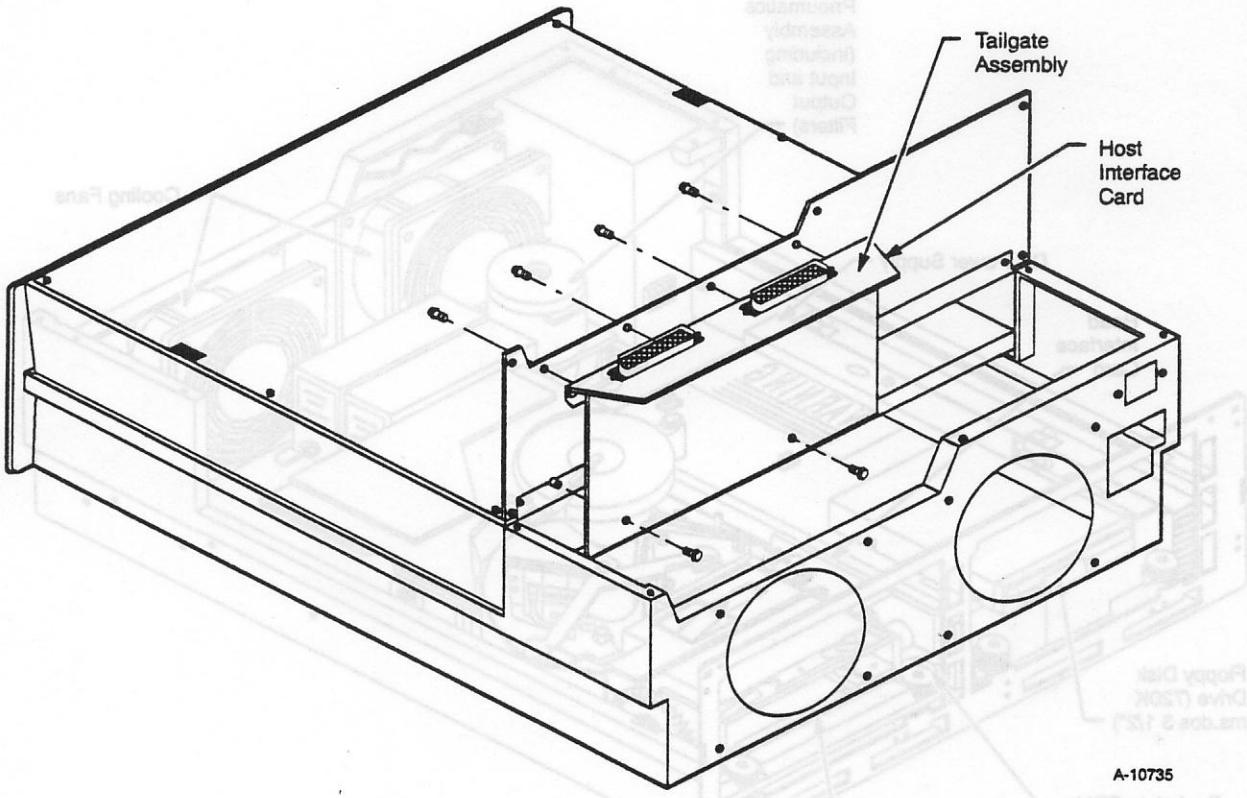


Figure 5-11. TD-3 Tape Drive Controller Module FRUs (Rear View)

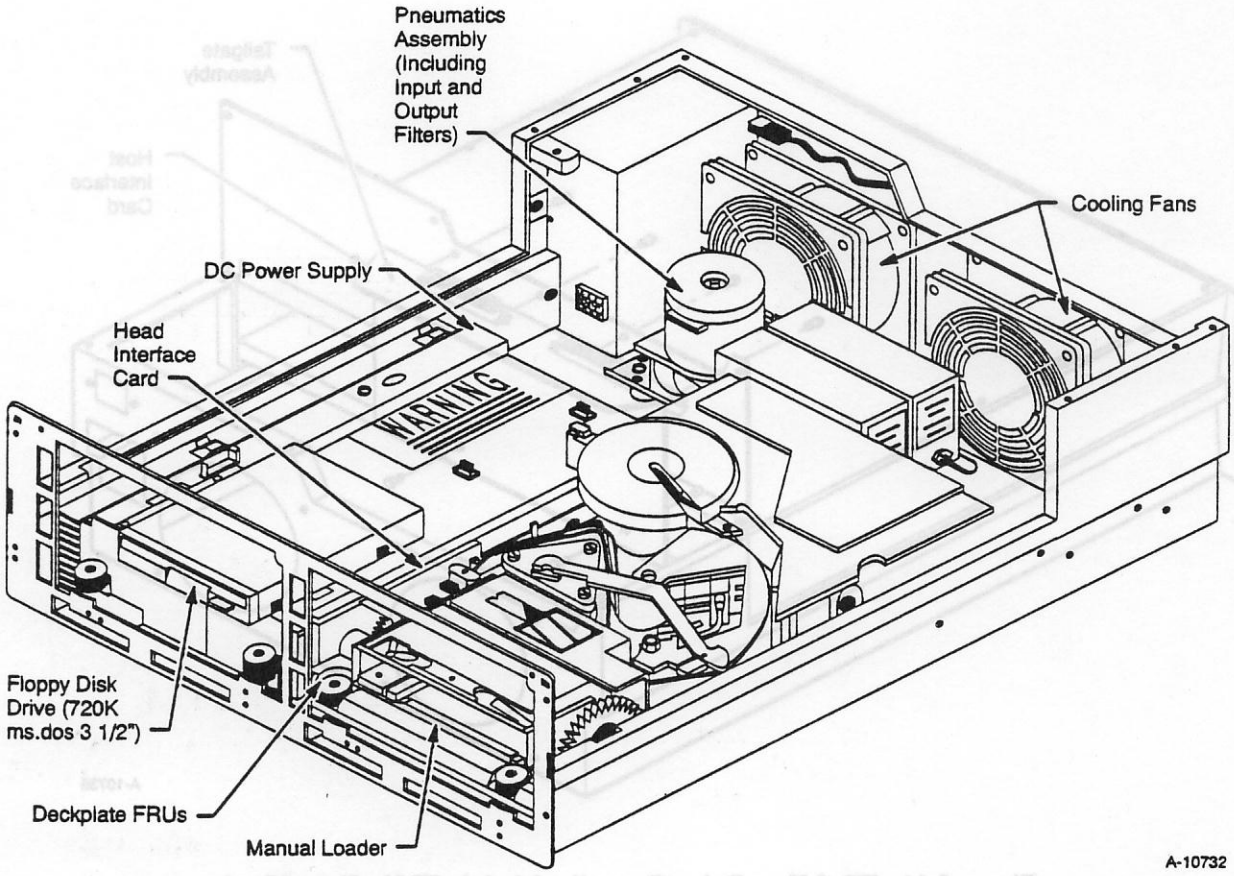


Figure 5-12. Drive Module FRUs

Disk Array Controller

The third non-FRU device in the CRAY Y-MP EL system peripherals is the disk array controller (DAC) unit supplied by Maximum Strategy, Inc. The DAC is an intelligent disk controller capable of storing and retrieving data from one to four banks of eight standard ESDI disk drives in parallel. The DAC also controls an additional drive for each bank of eight that is used to store a parity bit for fault protection as well as an operational standby (hot spare) drive used to replace a faulty drive from the bank.

The drives supported by the DAC are the DD-3, 5.25-in. ESDI serial data drives, capable of transferring data at a rate of 16 Mbytes/s in this configuration.

Each of the ten disk drives in the bank are connected to a disk interface and data buffer PC board in the DAC. The DAC also contains a parity PC board that is separate from the parity drive disk interface PC board, and a CPU PC board. The CPU contains a high-speed interface (HSI) unit. The DAC is designed to interface with up to four banks of ESDI drives. If more than one bank of drives is to be controlled, an additional HSI PC board must be installed for each bank. A multiplexer subassembly must also be installed to link the four banks to the one controller.

Figure 5-13 indicates which components must be removed to access the PC boards, and Figure 5-14 shows the location of each of the PC boards within the DAC.

The DAC has a small cut-out on the front panel (refer to Figure 5-13) in which the READY LED, a RESET button, and RS-422 serial communication (COM) port are visible. The READY LED is located on the CPU card in slot 12, and is a visual indicator of the state of the DAC. When the READY LED is glowing solid red, it indicates that the DAC is offline. During a normal power-on sequence or a reset sequence, the LED glows red as the disk drives spin up. The normal time for this sequence should not exceed 120 seconds. If the LED has not turned green after 120 seconds, it indicates a problem with the DAC or with one of the disk drives. Note in Figure 5-13 that each of the disk interface PC boards has an LED visible through the front shield. As the disk drive associated with the interface board spins up, this LED is red. When the disk drive is up to speed and when the internal diagnostics for the disk interface PC board have run, the LED turns green.

If the CPU READY LED is red, no communication is possible with the DAC. If any one of the data buffer/disk interface LEDs is red, either the disk drive failed to reach speed or the internal diagnostics for that interface board failed. In either case, the next step is to initiate disk drive diagnostics.

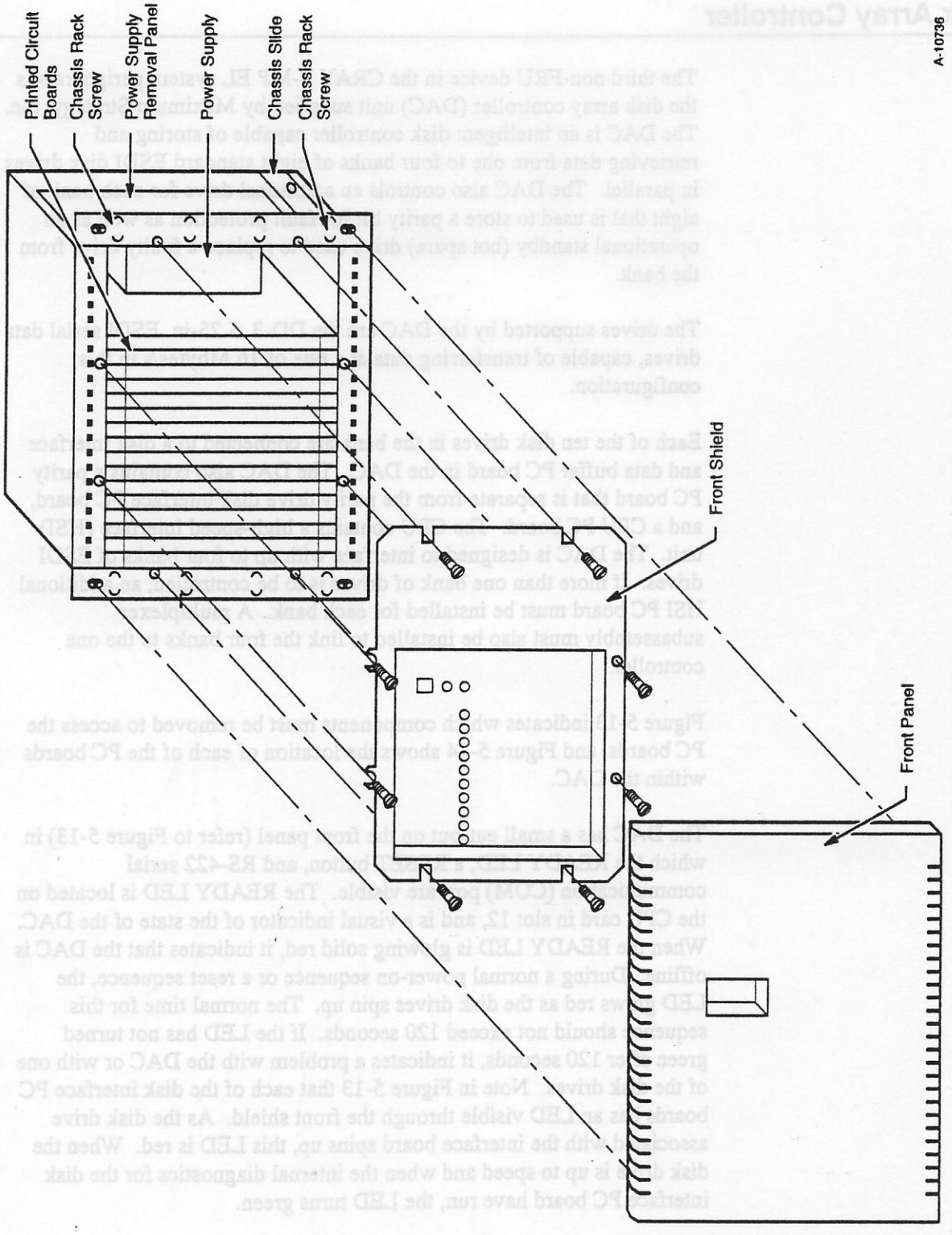
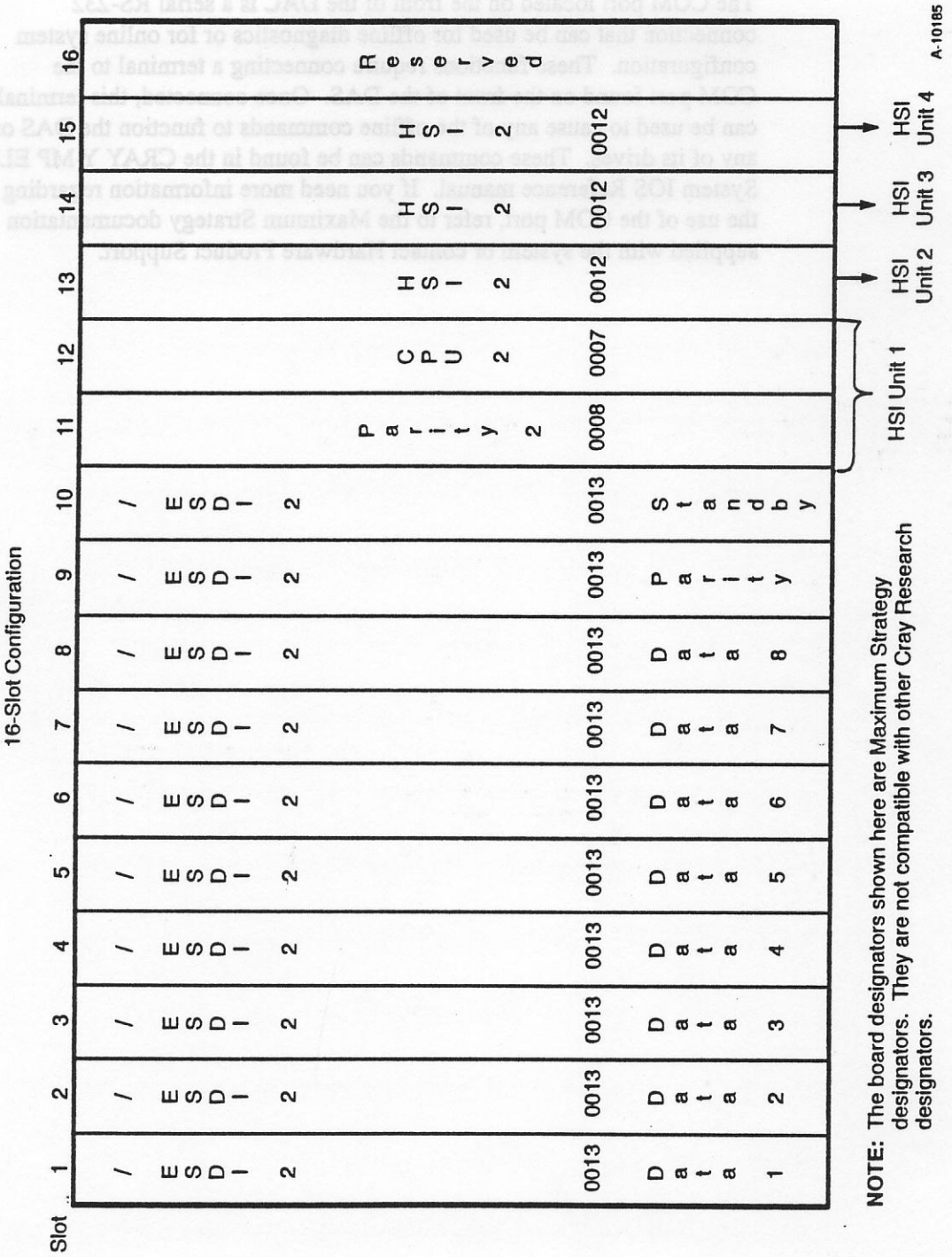


Figure 5-13. DAC Exploded View



NOTE: The board designators shown here are Maximum Strategy designators. They are not compatible with other Cray Research designators.

Figure 5-14. DAC Printed Circuit Board Locations

During normal operation, the RESET button should not be used. Instead, the reset function should be initiated by software through the IOS. However, during a power-up sequence you may use the RESET button once if the READY LED fails to turn green within 120 seconds.

The COM port located on the front of the DAC is a serial RS-232 connection that can be used for offline diagnostics or for online system configuration. These functions require connecting a terminal to the COM port found on the front of the DAS. Once connected, this terminal can be used to cause any of the offline commands to function the DAS or any of its drives. These commands can be found in the CRAY Y-MP EL System IOS Reference manual. If you need more information regarding the use of the COM port, refer to the Maximum Strategy documentation supplied with the system or contact Hardware Product Support.

6 POWER AND CONTROL SYSTEMS

Each of the cabinets that make up the CRAY Y-MP EL system maintains its own voltage distribution network. Each of the cabinets has its own AC input cord, but all of these cords are connected to circuit breakers at the rear of the primary cabinet in the Incoming AC Module (refer to Figure 6-1).

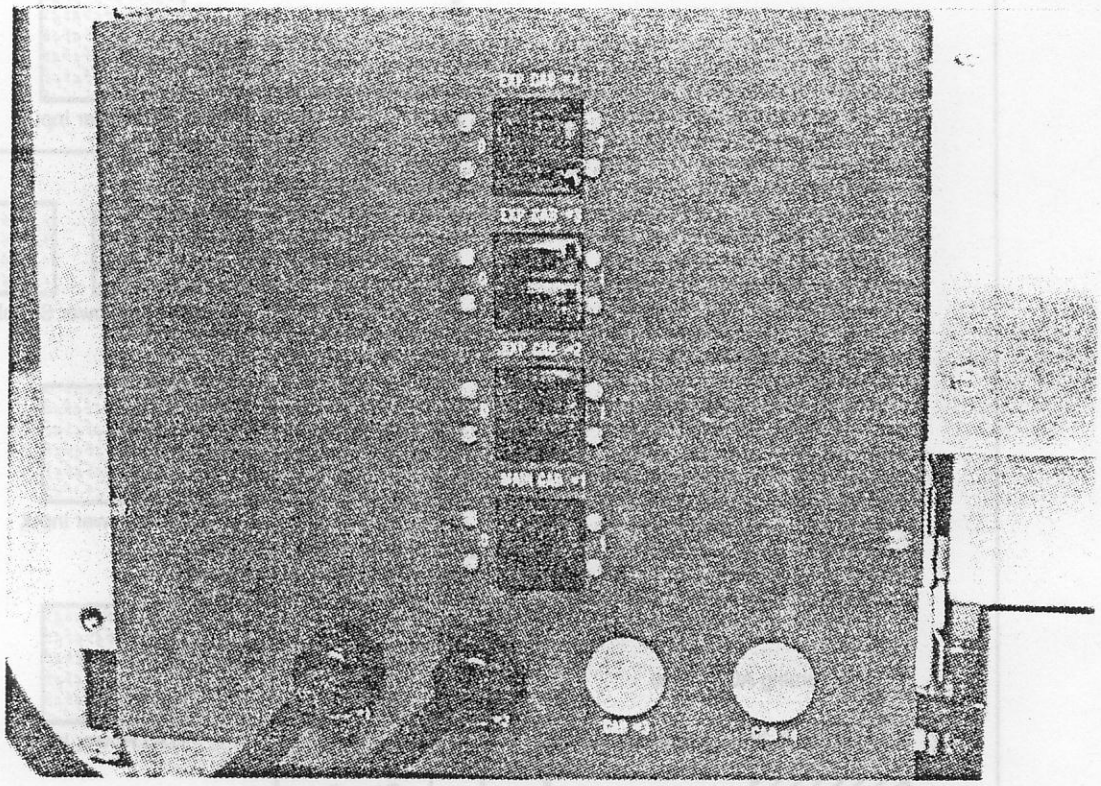


Figure 6-1. Incoming AC Module

The AC entering the CRAY Y-MP EL system is 208-Vac, single-phase, 50- to 60-Hz. After passing through the circuit breaker in the incoming AC module, the AC is next subjected to line filtering. The actual filtering takes place onboard a device called the capacitor ride-through module, but is not a function of the capacitor ride-through module. Refer to Figure 6-2 to trace the AC input.

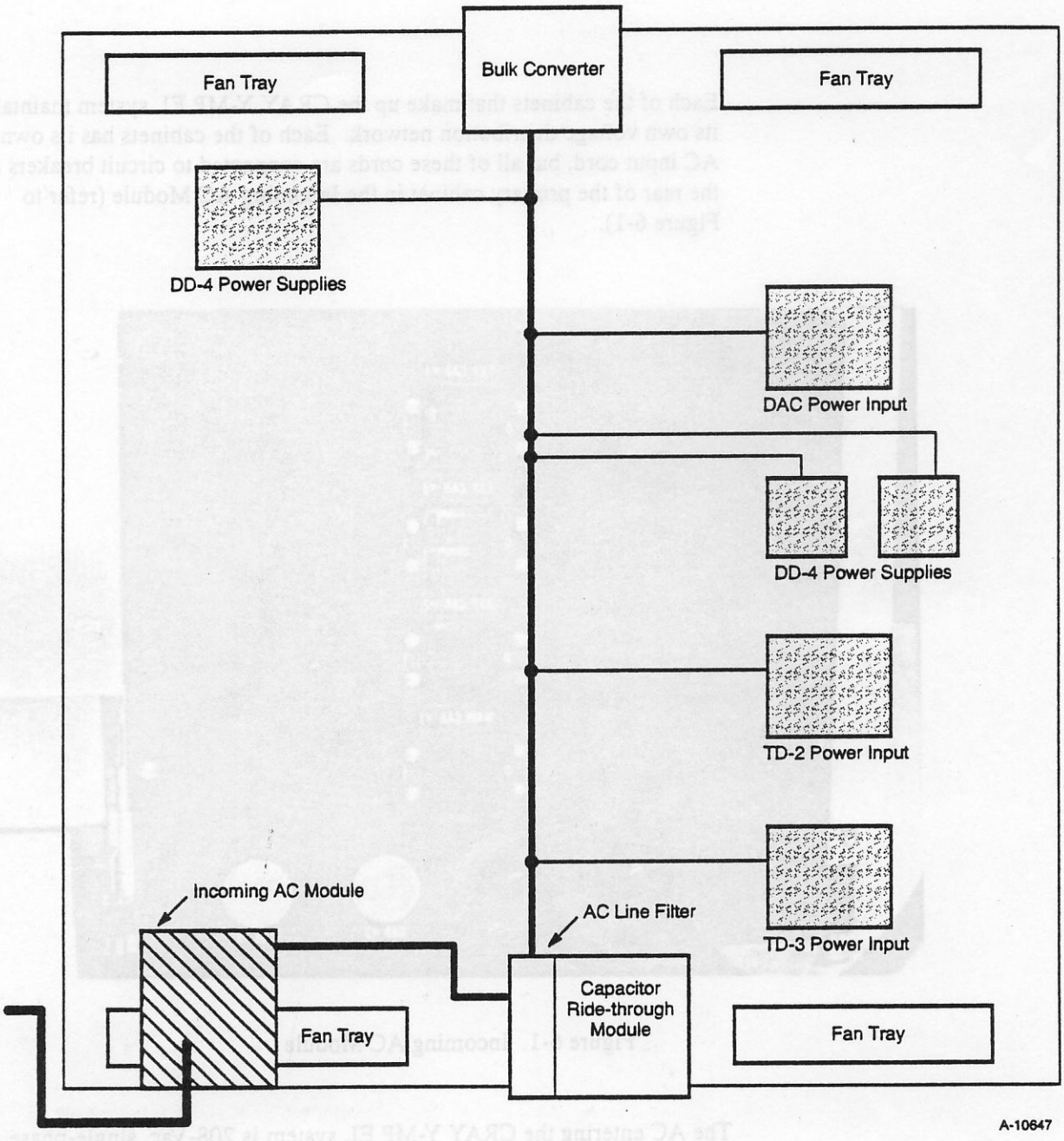


Figure 6-2. AC Distribution

After filtering, the AC input voltage is sent to a device called the bulk converter. The bulk converter is a module containing several power supplies, each of which is described in this section. As indicated in Figure 6-2 the 208 Vac can be tapped to run some of the peripheral devices. This provision is available at several levels along the power trace between the input line filter and the bulk converter because there is no fixed configuration for the CRAY Y-MP EL system peripherals. The AC input value is made available via three connector Molex-type plugs mounted as bulkhead connectors.

The CRAY ELS division has made every effort to standardize the wiring within the wiring trace so the product specialist will be able to recognize AC and DC wires without measurement. First, any green wire with a yellow stripe can be considered safety ground. It is always good practice to connect this wire first or to disconnect it last when performing maintenance that requires wiring. The CRAY Y-MP EL system has been designed so that the entire chassis will be safety grounded as long as the green/yellow wire remains connected.

NOTE: All wires dealing with high voltage values are double insulated.

The active high-voltage AC, or hot wire, within the CRAY Y-MP EL system is heavy gauge (14 to 16 ga.) black wire. Likewise, any high voltage DC is carried along heavy gauge red wires. It must be remembered that these wire color codes are CRAY ELS specific, selected by the Engineering department as an internal standard. There may be instances, when working with vendor equipment, that the product specialist could find red or black wires that do not conform to this color code.

DANGER

Wait for the system to completely power down before you touch any wire bundles. Bundles of heavy gauge black/green or red/green wire within the CRAY Y-MP EL system contain hazardous voltages. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

Voltage Hazards

380 Volts D.C.

Within the CRAY Y-MP EL system, there are generally four levels of voltage hazards. These levels are:

1. Safety Extra Low Voltage (SELV)

   It is safe to touch enabled connections carrying SELV levels of potential. This is commonly called signal voltage levels.

2. Extra Low Voltage (ELV)

   Mild electrical shock could result with contact. It can be dangerous to wear jewelry when working on equipment at this level of voltage.

3. High Voltage (HV)

   HV levels can cause severe electrical shock. Persons having physical problems (heart conditions, etc.) should practice extreme caution.

4. Tissue Damage Level (TDL)

   Extreme caution must be practiced. Contact could cause physical damage or death.

The CRAY Y-MP EL system has been designed so that all voltage levels are behind protective covers. To reach an open contact point of high voltage, it is necessary to remove the outer decorative cover; remove the inner Electro-magnetic Interference (EMI) cover; remove a contact or plug cover. Inside the peripheral drawers, only SELV or ELV values of power are present, and the top EMI cover must be removed to allow exposure. A further precaution is provided by the power connector used within the CRAY Y-MP EL system. This connector has the center (ground) prong longer than the other (power) connecters. This forces a condition of ground first on connect and ground last on disconnect, which adds a measure of protection to the process.

The operator will only be exposed to SELV levels of voltage hazard, as long as the operator does not remove an inner protective cover. The product specialist, after removing the protective covers, will be exposed to ELV and HV levels of hazard. Normal protective measures should be observed. The only places that TDL values of hazard can be encountered are inside the bulk converter module, the capacitor ride-through module, and the incoming AC module. Removing the covers from these devices is discouraged and dangerous because in the case of the bulk converter and the capacitor ride-through modules, this action will void the manufacturer's warranty.

Inside the bulk converter module, the input AC is applied to the input side of a pair of 12-Vdc power supplies. The outputs of these two supplies provide the 12 Vdc required to operate the fans for the cooling system in the CRAY Y-MP EL system. As shown in Figure 6-3, each 12-V supply feeds two fan trays, one bottom and one top. Also note that the fan trays supplied by each power supply are in opposite diagonal corners of the chassis. The reason for this placement is that a cooling chimney can be operated with only one fan tray. If a problem occurs in a fan power supply, only one fan tray in each chimney will be halted, allowing the CRAY Y-MP EL system to continue operation until repairs can be initiated.

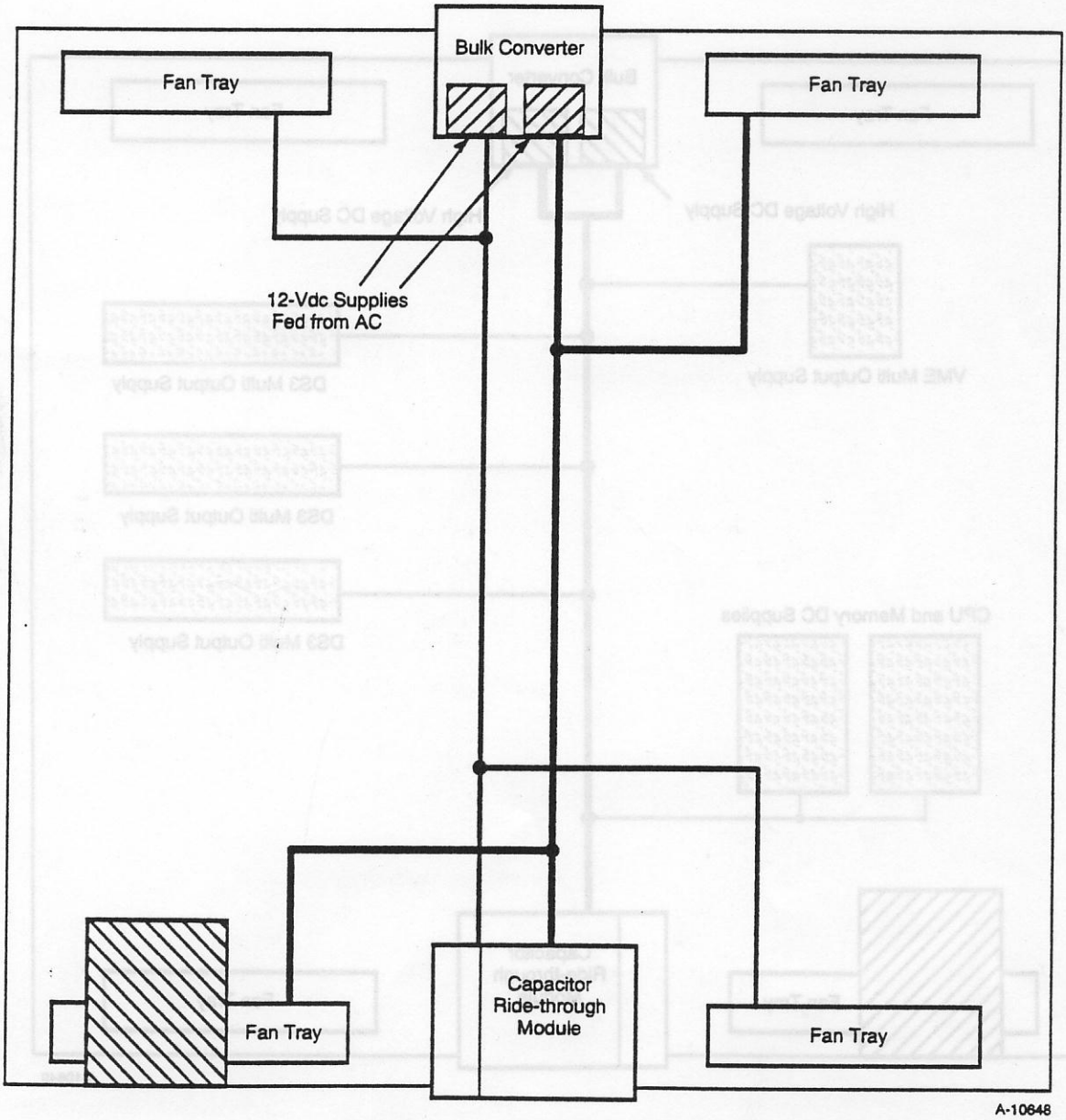


Figure 6-3. 12-Vdc Distribution

The fans used in the fan trays of the CRAY Y-MP EL system are DC muffin fans. There are nine fans in each of the fan trays, and the fans are connected to a self-monitoring system. If any one fan should fail in a fan tray, the entire fan tray will stop operating and the appropriate LED on the monitor panel will illuminate.

The bulk converter module also contains two 380-Vdc power supplies, as shown in Figure 6-4. These power supplies provide the DC necessary to operate the main components of the CRAY Y-MP EL system. In most cases, as noted in Figure 6-4, this high-voltage DC is the input to specific local power supplies within the various subassemblies of the CRAY Y-MP EL system.

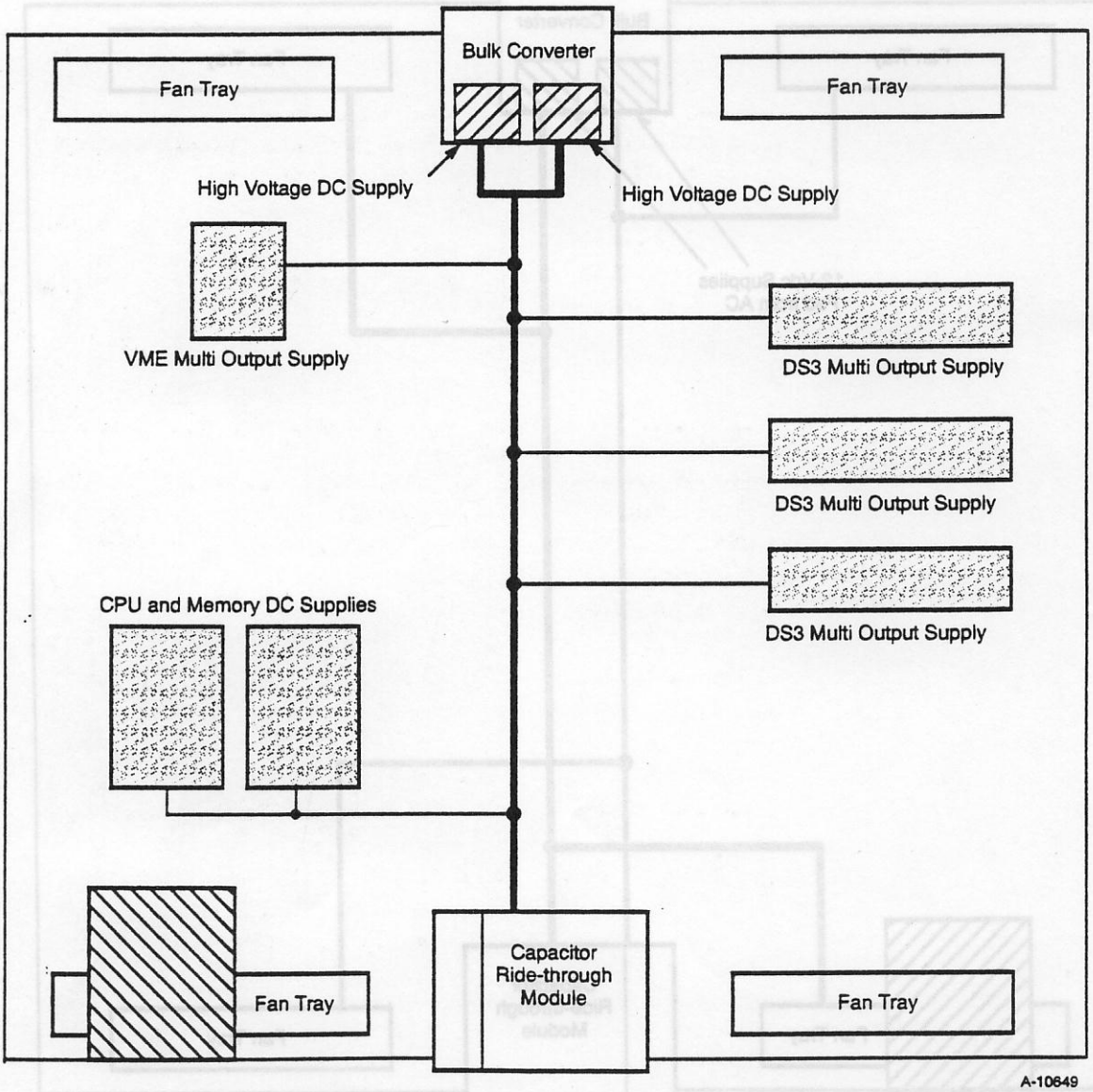


Figure 6-4. High-voltage DC Distribution

The high-voltage DC is supplied within the wire trace by means of 4-position mate and lock connectors. These connectors are available at the various peripheral drawer levels, allowing the configuration versatility that is one of the primary advantages of the CRAY Y-MP EL system. These DC connectors are all deep contact connectors to provide maximum protection to the product specialist.

As can be seen in Figure 6-3 and Figure 6-4, the 12-Vdc and 380-Vdc power supplies also input their voltages into the capacitor ride-through module. This module is designed as a large storage container that can be used to supply power in case of momentary AC line faults. The capacitor ride-through module, as its name implies, is primarily a bank of capacitors in a sealed box, thus its more common name, the capacitor box. This capacitor box is designed to maintain the 12 Vdc power and the 380-Vdc power for up to 10 seconds, depending on load.

The capacitor box is disabled when the CRAY Y-MP EL system is shut off. The circuit breakers located on the incoming AC module have a shunt switch that is engaged when the circuit breaker is placed in the OFF position. This shunt switch is directly connected across the capacitor box output, providing a short circuit to the capacitors when it is engaged. This shunt completely and instantaneously discharges the capacitors to protect the operator and the product specialist from potentially fatal injury.

Control

The control of the CRAY Y-MP EL system is a minor function of the product specialist. All of the voltage values are fixed, with some specified allowable tolerances. Even during preventive maintenance periods, voltage values are not changed. You can change the output values of the CPU power supply and the memory power supply as a tool in isolating intermittent faults. The voltage adjustment potentiometers are located behind the pull-down door on the bottom of the front indicator panel, as shown in Figure 6-5.

There are several other controls located on the control panel that are accessible by opening the pull-down door. One of these is a square button labeled SYSTEM OFF. This control can be located using Figure 6-5. Pressing the SYSTEM OFF button produces a momentary short circuit across each of the main circuit breakers being used on the incoming AC module, forcing them to trip, and resulting in a removal of AC input voltage. This button is the recommended method of removing power from the system in a normal power-down operation.

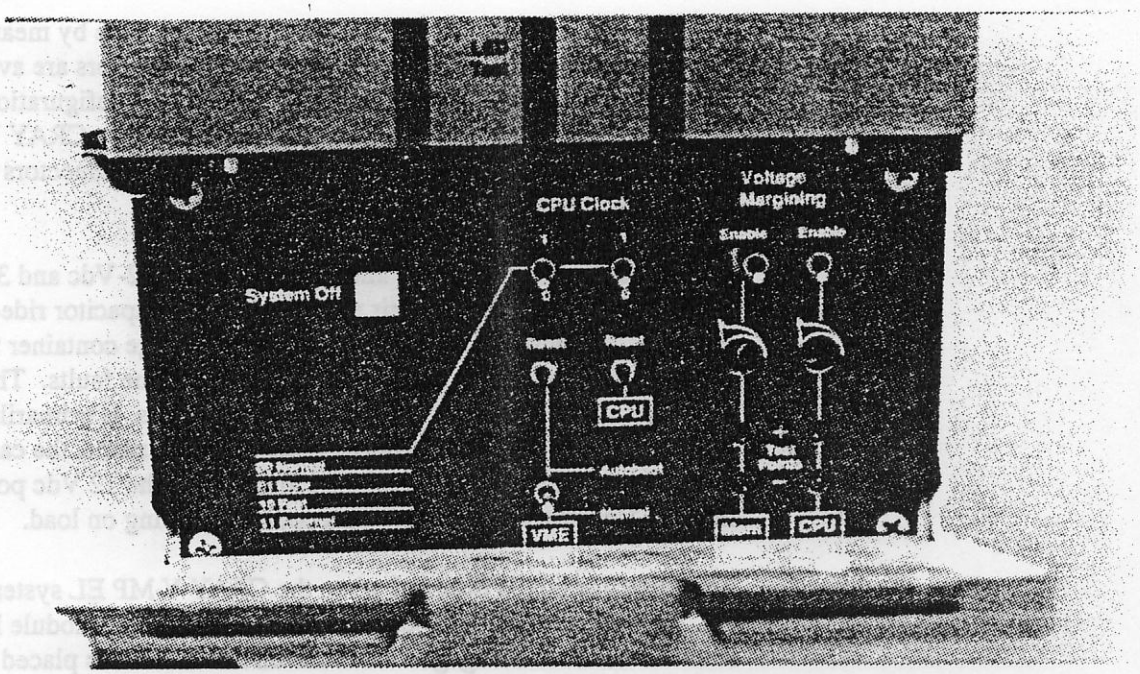


Figure 6-5. Control Panel Door

Other control devices located on the control panel include two reset buttons, one for the VME and one for the CPU. These buttons, when depressed, cause a hard disconnect and reconnect of the associated subassemblies. This hard disconnect forces the associated subassembly to start over at ground zero, just as if the system had been disconnected from the incoming AC, then reconnected. Depressing these buttons terminates any processes running in the CPU on the VME.

Another set of controls on the control panel consists of two toggle switches that are used in combination to set the internal clock speed. The clock switches are provided as a troubleshooting tool to be used in case of intermittent faults. The switches can be set to fast clock, which does not appreciably increase the performance of the CPU. This point must be made clear to operating personnel, as the controls are accessible to them. The two switches that change the clock to predetermined settings are used as binary bits, providing settings of:

- 00 – normal
- 01 – slow
- 10 – fast
- 11 – external

The final control on the front of the CRAY Y-MP EL system is the emergency power-off (EPO) button, shown in Figure 6-6. As its name implies, this button is provided for use in an emergency situation. Depressing this button causes a short circuit across the AC circuit

breakers on the incoming AC module, causing them to trip and disconnect the AC input voltage. The EPO is a push and lock device; once depressed, the short circuit is maintained across the AC circuit breakers, preventing reconnection of the incoming AC voltage.

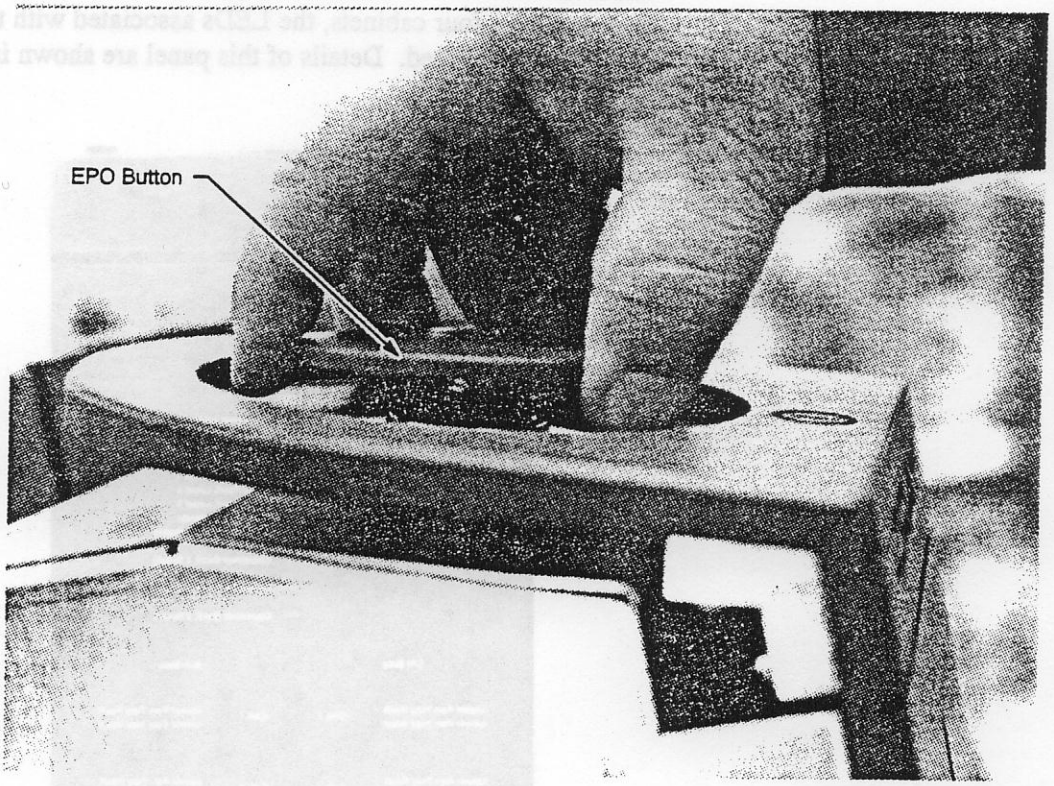


Figure 6-6. EPO Button

When the emergency has been dealt with and it is again safe to apply power to the CRAY Y-MP EL system, it is necessary to remove the short circuit across the circuit breakers. The EPO button is a twist-to-unlock device. When you twist the EPO approximately 1/8 turn counter-clockwise, the locking mechanism is released, the EPO returns to its normal position, and the short circuit is removed from the AC circuit breakers allowing a normal power-up sequence.

The normal power-up sequence of the CRAY Y-MP EL system is quite simple. All that is required is to turn on the appropriate circuit breakers on the incoming AC module, one for each cabinet in the system.

Monitoring

A front-mounted LED panel, shown in Figure 6-7, monitors conditions in the CRAY Y-MP EL system. The monitor panel consists of amber and green LEDs connected to various subassemblies. The monitor panel contains LEDs for a four-cabinet system. If the system being monitored does not have four cabinets, the LEDs associated with the missing cabinets are not used. Details of this panel are shown in Figure 6-8.

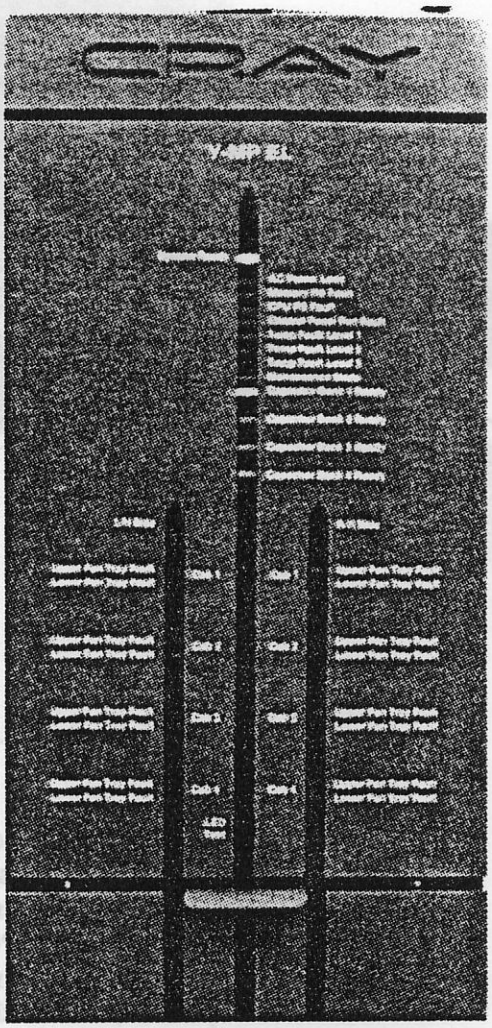


Figure 6-7. Control Panel

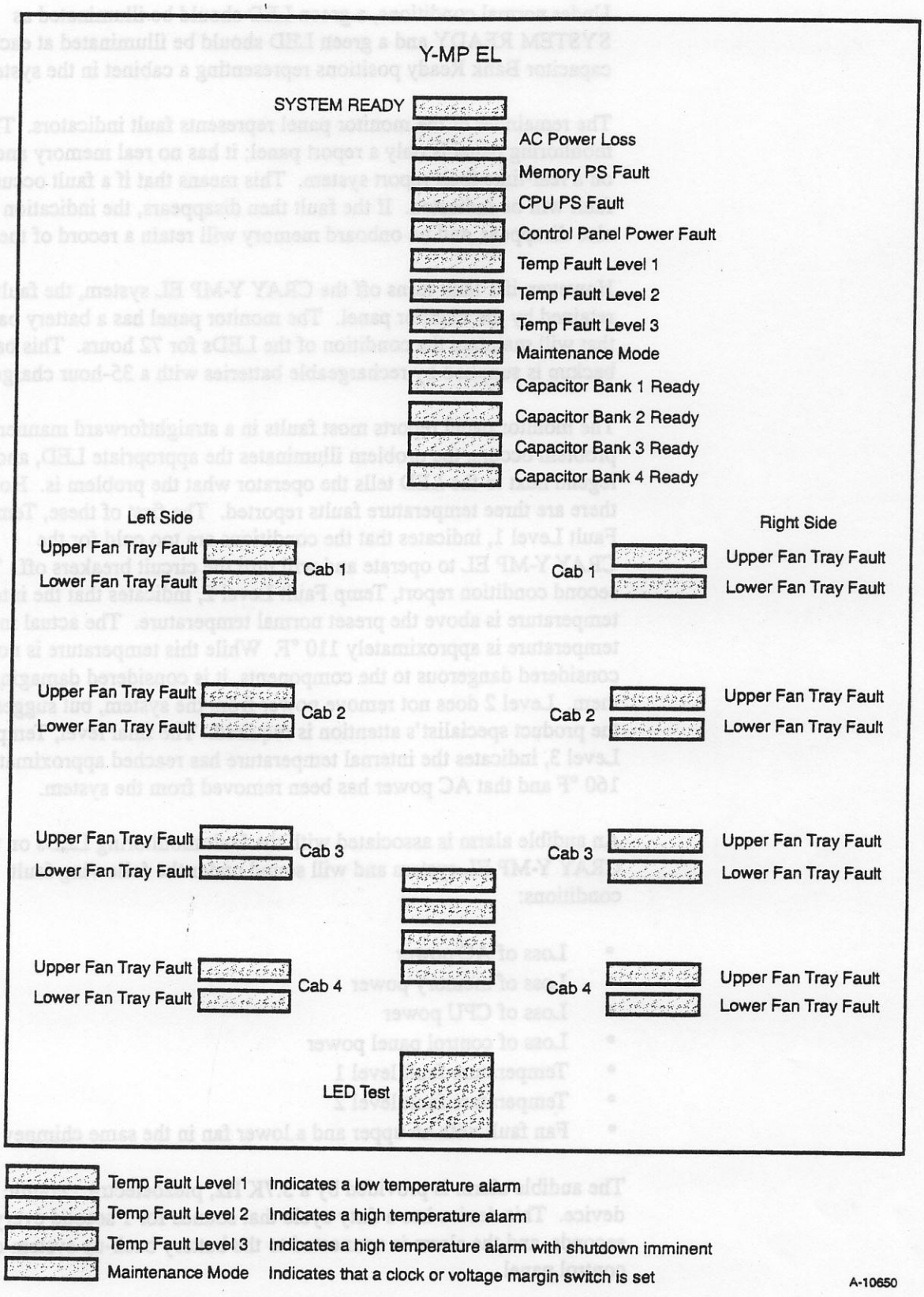


Figure 6-8. Control Panel Warning and Ready Indicators

Under normal conditions, a green LED should be illuminated as SYSTEM READY and a green LED should be illuminated at each of the capacitor Bank Ready positions representing a cabinet in the system.

The remainder of the monitor panel represents fault indicators. This monitoring panel is only a report panel; it has no real memory and runs on a real-time fault report system. This means that if a fault occurs, the fault will be indicated. If the fault then disappears, the indication will also disappear, and no onboard memory will retain a record of the fault.

However, if a fault turns off the CRAY Y-MP EL system, the fault is retained by the monitor panel. The monitor panel has a battery backup that will maintain the condition of the LEDs for 72 hours. This battery backup is supplied by rechargeable batteries with a 35-hour charge cycle.

The monitor panel reports most faults in a straightforward manner. If a problem occurs, the problem illuminates the appropriate LED, and the legend next to the LED tells the operator what the problem is. However, there are three temperature faults reported. The first of these, Temp Fault Level 1, indicates that the conditions are too cold for the CRAY Y-MP EL to operate and will turn the circuit breakers off. The second condition report, Temp Fault Level 2, indicates that the internal temperature is above the preset normal temperature. The actual internal temperature is approximately 110 °F. While this temperature is not considered dangerous to the components, it is considered damaging to them. Level 2 does not remove power from the system, but suggests that the product specialist's attention is required. The final level, Temp Fault Level 3, indicates the internal temperature has reached approximately 160 °F and that AC power has been removed from the system.

An audible alarm is associated with the fault monitoring LEDs on the CRAY Y-MP EL system and will sound under the following fault conditions:

- Loss of AC power
- Loss of memory power
- Loss of CPU power
- Loss of control panel power
- Temperature fault level 1
- Temperature fault level 2
- Fan fault with an upper and a lower fan in the same chimney

The audible alarm is provided by a 3.7K Hz, piezoelectric ceramic device. This device has a duty cycle that sounds for 1 second every 10 seconds, and the alarm is connected to the battery back-up system on the control panel.

The maintenance mode LED is a warning light that illuminates whenever any of the condition-altering controls are used. The controls monitored are the CPU margin switch, the memory margin switch, and the clock speed switches. Changing any of these controls from their normal condition illuminates the maintenance mode LED.

The SYSTEM READY LED is illuminated when six conditions are met. They are:

- Incoming AC
- CPU voltage good
- Memory voltage good
- +12 Vdc good
- All capacitor banks are above 200 Vdc
- Three-minute timer has expired

7 FIELD REPLACEMENT PROCEDURES

This section describes the field replacement procedures (FRPs) to follow when you perform maintenance activities on the CRAY Y-MP EL system. When you perform maintenance, always observe all safety precautions and electrostatic discharge (ESD) prevention guidelines.

Dangers, Warnings, and Cautions

Hazard statements advise maintenance personnel of dangers they may encounter while servicing Cray Research equipment. The following list describes the hazard statement signal words.

- Danger – Indicates an imminently hazardous situation that, if not avoided, will result in death or serious injury.
- Warning – Indicates a potentially hazardous situation that, if not avoided, could result in death or serious injury.
- Caution – Indicates a potentially hazardous situation that, if not, avoided, may result in minor or moderate injury. This signal word is also used to alert personnel against unsafe practices that can result in machine damage and/or data corruption.

Safety Precautions

Observe the following safety precautions when you perform maintenance on the CRAY Y-MP EL system.

1. Do not move the cabinets while they are connected to power.
2. Do not wear watches, necklaces, or other jewelry when working inside a CRAY Y-MP EL system cabinet.

WARNING

Severe shock and burns as well as short circuits can occur when you wear rings, watches, or other jewelry during this procedure. Remove all jewelry before starting this procedure. Observe the ESD precautions described in this section.

3. Keep fingers and conductive tools away from high-voltage areas, such as the CRAY Y-MP EL capacitor bank and bulkhead as well as the high-current areas on the CPU, memory, or VME IOS power supplies or buses.

DANGER

The CRAY Y-MP EL capacitor bank and bulkhead contain a potential 380 volts. Keep fingers and conductive tools away from these high-voltage areas. Perform a voltage check on the system before attempting any maintenance. Serious injury or death will occur if these precautions are not followed.

4. All circuit breakers should be in the OFF (0) position before plugging in the power cord.

5. Ensure that all items removed from the system during servicing are replaced (covers, tools, etc.) when finished.

6. Disconnect the main power plug from the system before working on the power system (capacitor bank and bulkhead).

CAUTION

Depressing the emergency power-off button will immediately shut down the system. Customer data may be lost. Follow shut-down procedure whenever possible.

ESD Precautions

Observe electrostatic discharge precautions during the installation process. Required apparel includes an ESD smock, ESD wrist strap, ESD shoes, and a static mat.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment may result if these precautions are not followed.

ESD Smock

Wear a Cray Research-approved static-dissipative smock when servicing or handling an ESD-sensitive device. Completely button the smock and wear it as the outermost layer of clothing. You must have a portion of the smock's sleeves in direct contact with the skin of your arms. Skin contact is essential for a dissipative path-to-earth ground through your wrist strap. Tuck hair exceeding shoulder length inside the back of the smock.

Wrist Strap

Wear a Cray Research-approved wrist strap when servicing or handling an ESD-sensitive device. Connect the wrist strap cord directly to earth ground to reduce ESD damage to equipment.

ESD Shoes

Wear static-dissipative shoes or shoes with heel straps on both shoes when servicing or handling an ESD-sensitive device. When sensitive equipment is exposed to static discharge, ESD shoes provide an effective backup to the wrist straps and grounding cords.

FRP1

Powering Up the CRAY Y-MP EL System

The power-up procedure is done on the circuit breaker panel on the rear of the CRAY Y-MP EL system. There will be up to a 3-minute delay before the power light emitting diodes (LEDs) illuminate on the control panel.

Procedure

1. Ensure that the AC power plug is connected to power.
2. Ensure that the AC POWER LOSS LED is illuminated on the control panel. Refer to Figure 7-1.
3. Ensure that the emergency power off (EPO) button, located on the control panel, is extended outward by turning it counterclockwise to the stop. If it is in, it will now pop out. Refer to Figure 7-2.
4. Ensure that all individual components are powered on at this time. The locations of power-on buttons are as follows:
   a. The CPU and memory (MEM) buttons are located above the CPU and memory boards on the CPU card cage.
   b. The IOS Enable/Inhibit button is located above the IOS VME card cage.
   c. The individual peripheral equipment drawers each have a power supply enable button located on the front of the drawer.
5. Move the circuit breakers on the back of the mainframe cabinet to the ON position (1). Refer to Figure 7-3.
   a. Visually inspect to ensure that there is no sparking or smoking among the components once you have powered up the system.
6. Ensure that the fans are operating.
7. Ensure that the capacitor bank LED is illuminated for each cabinet on the control panel. Refer again to Figure 7-1. This takes approximately 1 minute.

8. The control panel System Ready LED will illuminate in approximately five minutes, after everything is initiated.

9. Ensure that the maintenance workstation model EL (MWS-EL) and the system console are powered on.

NOTE: The **`courier bold`** font indicates commands, options, and field inputs that the user should enter.

10. The MWS-EL or system console boot prompt should appear on the IOS screen (window). Type **`load`** at the boot prompt. The system will go through its initializing program upon receiving the IOS prompt.

11. Load UNICOS. Refer to *UNICOS 6.1 System Installation Bulletin for Cray Research Entry-level (EL) Systems*, CRI publication number SG-5201.

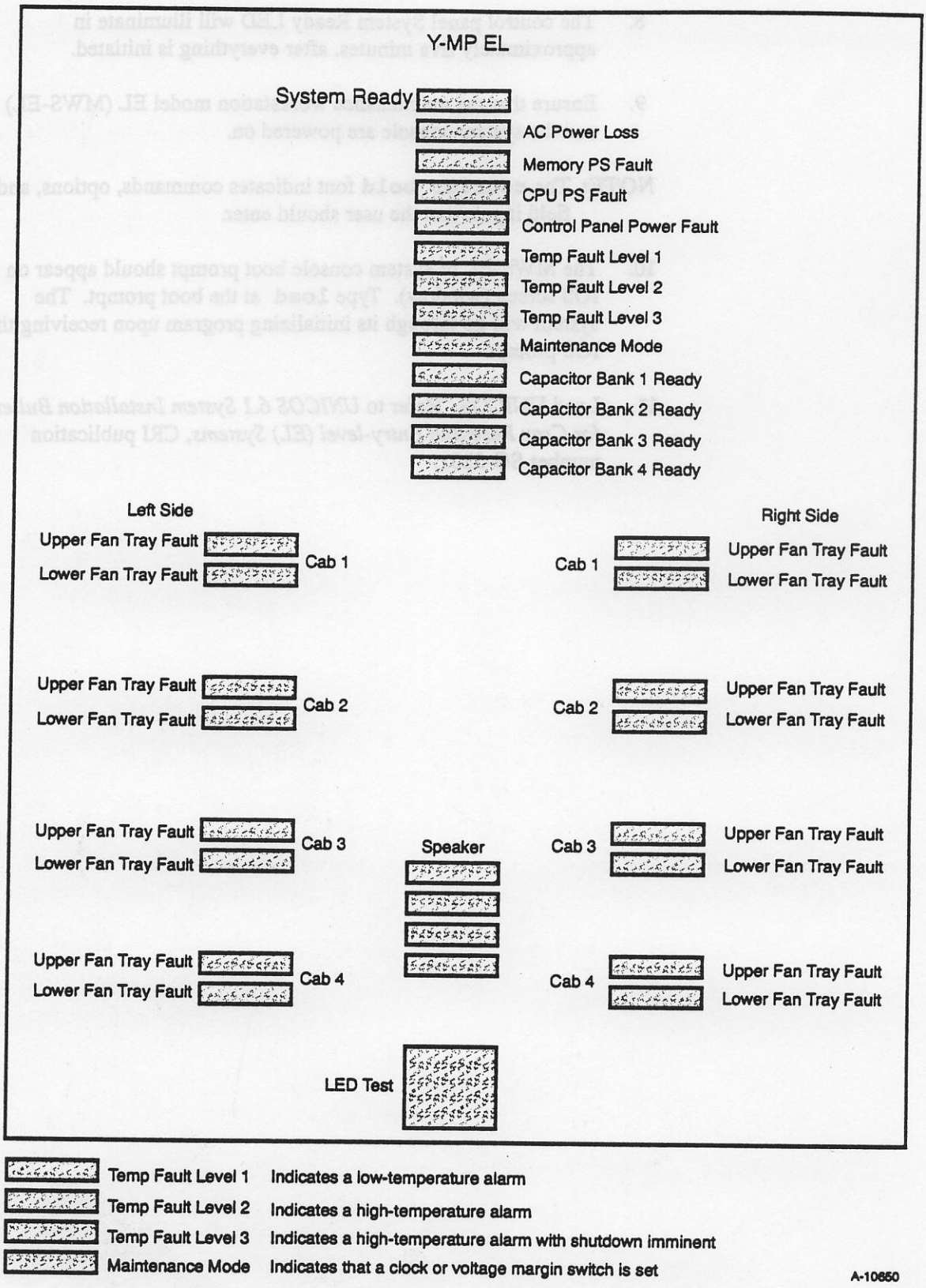


Figure 7-1. CRAY Y-MP EL Control Panel LEDs

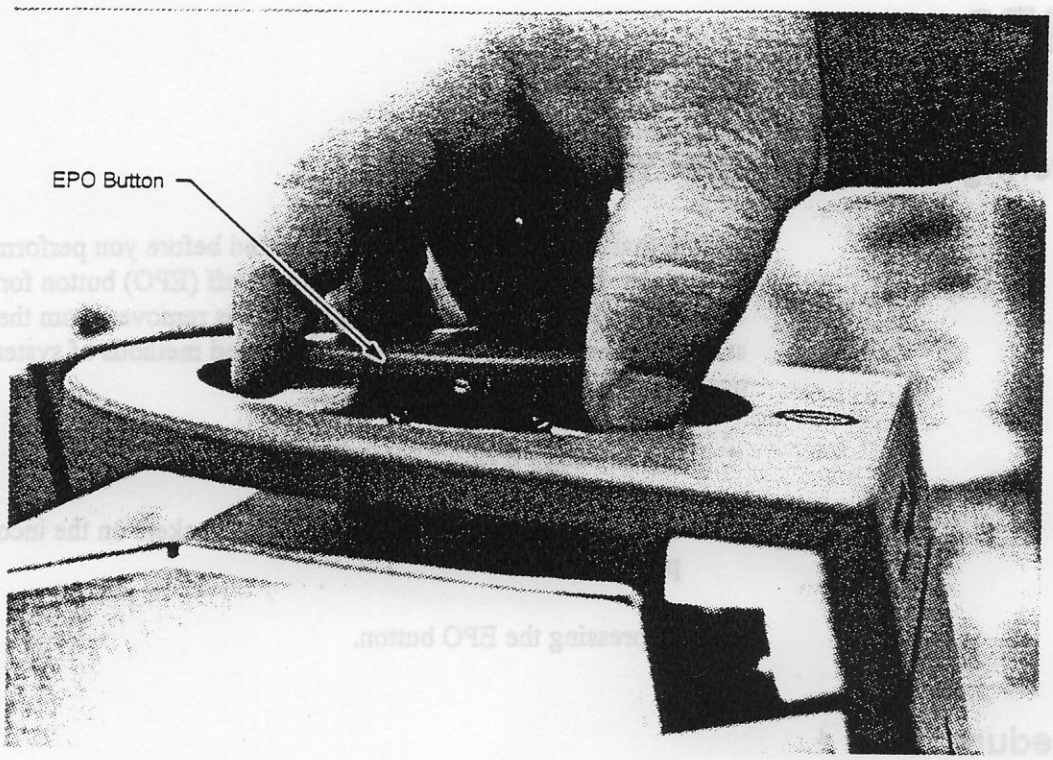


Figure 7-2. EPO Button

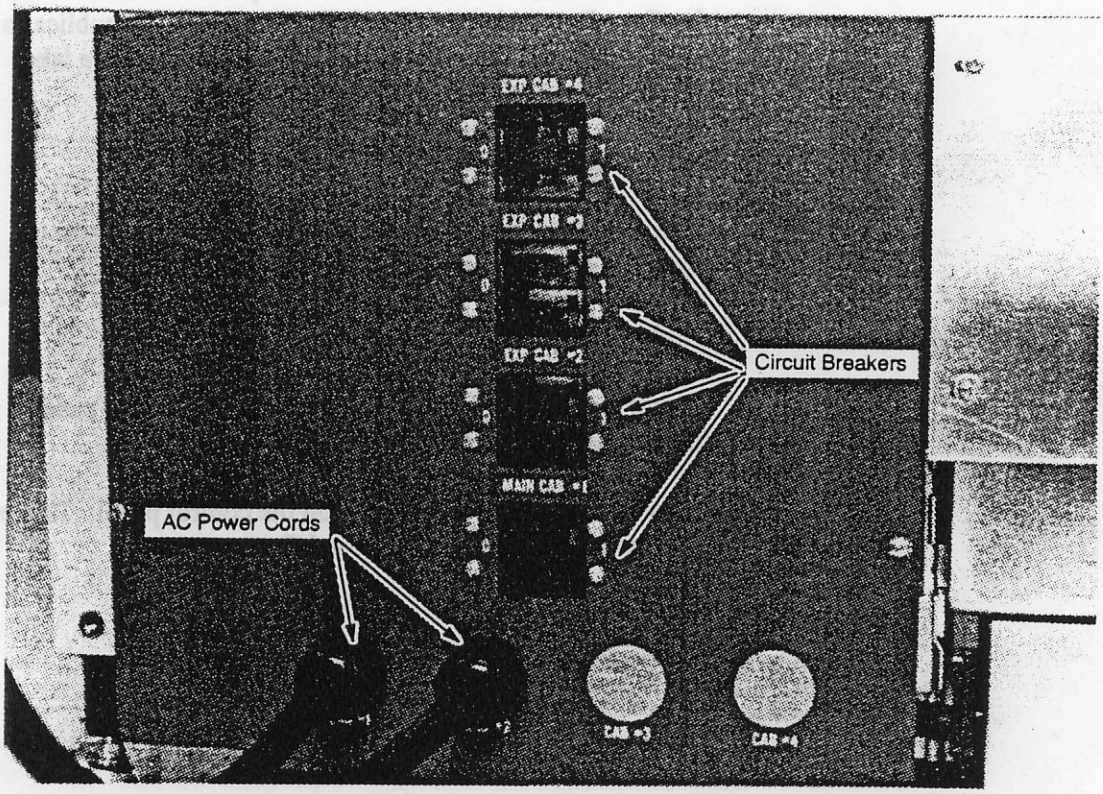


Figure 7-3. CRAY Y-MP EL Circuit Breakers

FRP2

Powering Down the CRAY Y-MP EL System

Ensure that all customer jobs are completed before you perform this procedure. Depress the emergency power-off (EPO) button for all types of maintenance; this ensures that all power is removed from the system and will remain powered off. Three accepted methods of system power-down are

- Performing FRP2.
- Turning off individual cabinet circuit breakers on the incoming power module.
- Depressing the EPO button.

Procedure

1. On the maintenance workstation model EL (MWS-EL), unmount UNICOS. Refer to the *UNICOS 6.1 System Installation Bulletin for Cray Research Entry-level (EL) Systems*, CRI publication number SG-5201, for this procedure. This procedure takes approximately 15 minutes.
2. Depress the EPO button.
3. Turn off (0) the circuit breakers for each cabinet. Refer to Figure 7-3 for a photograph of the circuit breakers.
4. Unplug the system from the AC power source.
5. Ensure that the AC Power Loss LED on the control panel is now illuminated. Refer to Figure 7-1.
6. Press the SYSTEM OFF button on the control panel. This button is located behind the control panel flap.

FRP3

Removing the Front Panel Assembly

This procedure requires two people.

Procedure

1. Release the lower two spring catches at the bottom of the front panel (there is one located in each corner) and push up. Refer to Figure 7-4. The bottom of the panel has now been released and is hanging from the panel mounting screw. Refer to Figure 7-5.

2. Position one person at each end of the panel to lift the panel and ease it upward and outward, while taking care not to damage the control board trim cover. Be careful not to push the emergency power-off (EPO) button.

3. Remove the inner front panel electromagnetic interference (EMI) shield by removing the four screws located near the middle of the EMI shield as shown in Figure 7-6.

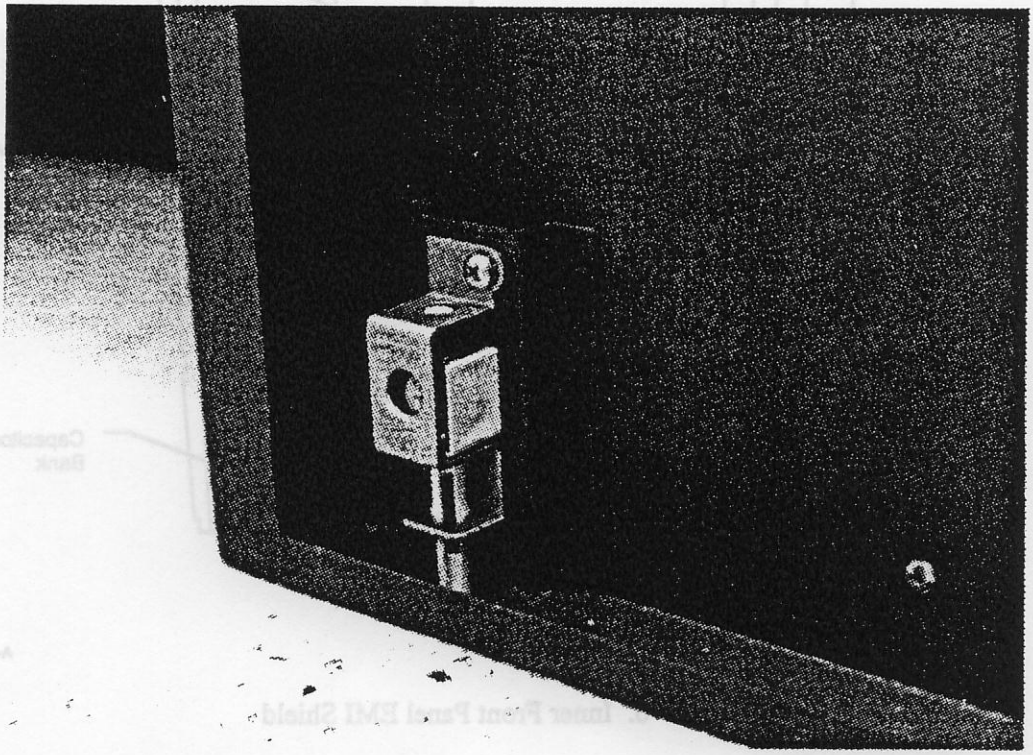


Figure 7-4. Front Panel Spring Catches

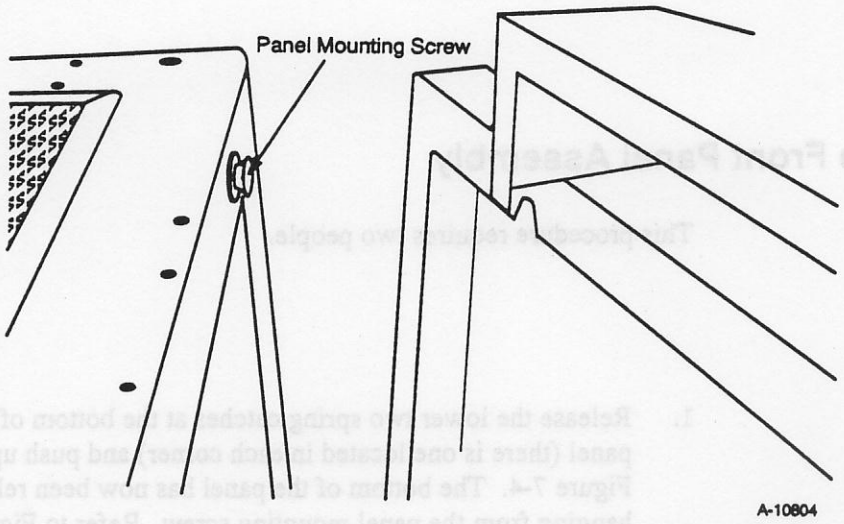


Figure 7-5. Panel Mounting Screw

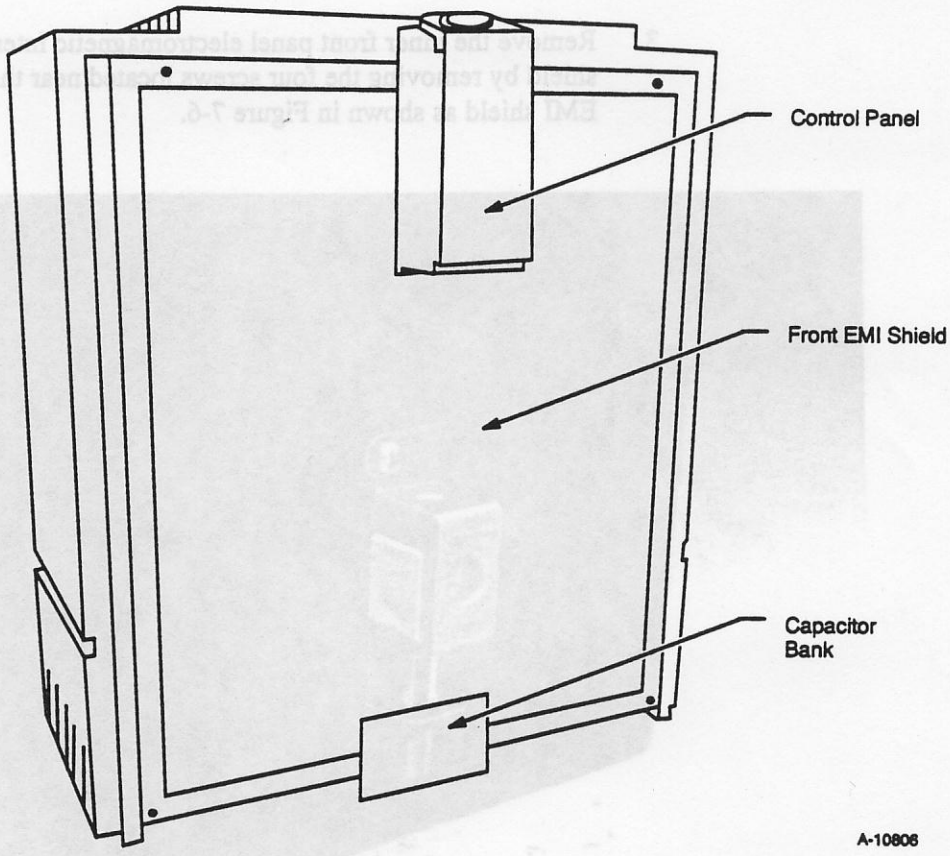


Figure 7-6. Inner Front Panel EMI Shield

FRP4

Replacing the Front Panel

This procedure requires two people.

Procedure

1. Replace the inner front panel EMI shield (Figure 7-6) by placing the panel correctly back into the frame and securing the four panel screws.

2. Hang the panel on the panel mounting screw carefully. Refer to Figure 7-5. Be careful not to damage the control board trim cover.

3. Push the bottom of the panel into the frame; you should hear a click as the panel locks into position.

FRP5

Opening or Removing the Side Panels

This procedure applies to both the left and right side panels. A few of the procedures require you to actually remove the side panel. If you are removing a right side panel, you will have to remove the front panel assembly first. If you are removing a left side panel on a single cabinet system, you will have to remove the back panel assembly first.

Procedure

1. Turn the latch (Figure 7-7) counterclockwise one full turn to unlatch and swing the panel open.

NOTE: Proceed to Step 2 only if the procedure you are performing indicates that a side panel should be removed.

2. Lift the panel upward, keeping it as straight as possible until it clears the hinge pins.

3. Adjust the latch with a 3/8-inch wrench.

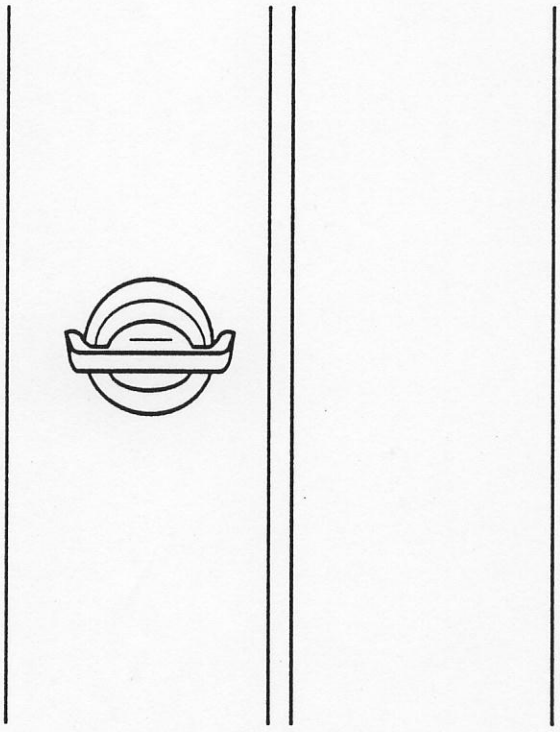


Figure 7-7. Side Panel Latch

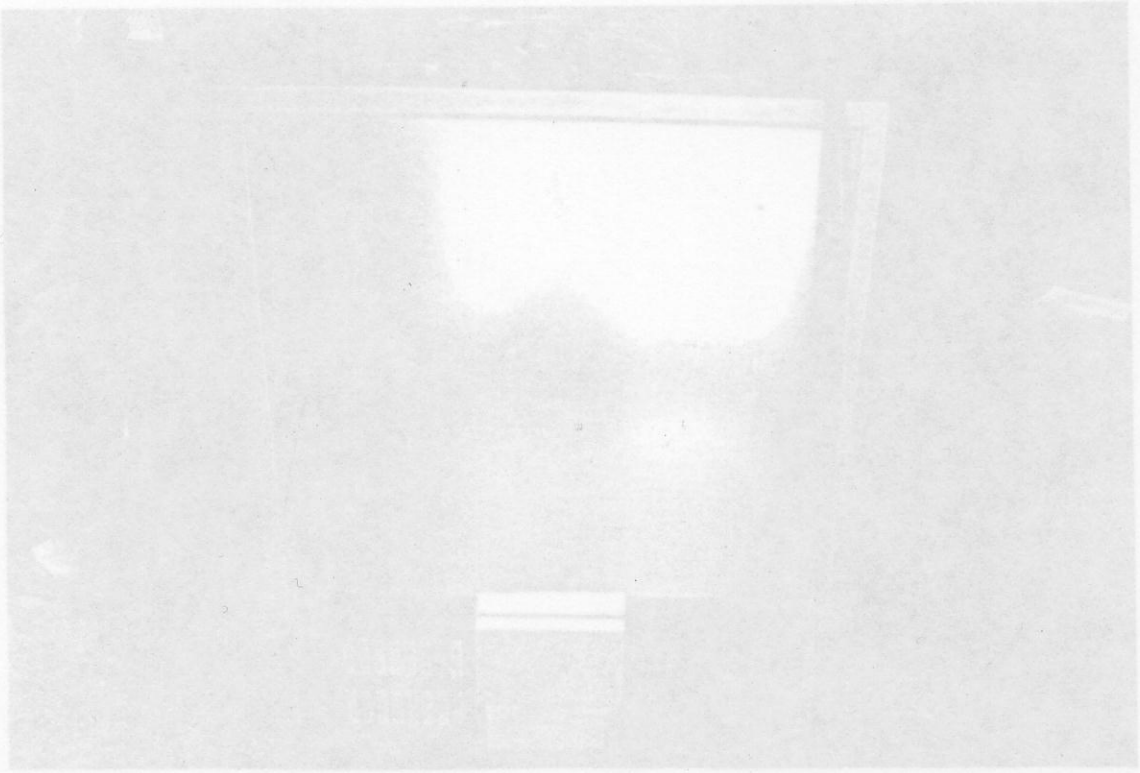
FRP6

Closing or Replacing the Side Panels

If the procedure you are performing indicates that the panel needs to only be opened, use Step 2 to shut either panel.

Procedure

1. Carefully lower the panel onto the hinge pins.
2. Push the panel to close it, and turn the latch clockwise until it locks. Refer to Figure 7-7.



FRP7

Removing the Back Panel Assembly

This procedure includes removing the back panel and the inner back panel EMI shield. Removing the back panel requires two people.

Procedure

1. Release the lower two spring catches (Figure 7-4) located on the bottom of the panel (there is one located in each corner) and push up on the release rod. The bottom of the panel has now been released and is hanging from the panel mounting screw. Refer to Figure 7-5.

2. Position one person at each end of the panel to lift the panel and ease it outward.

3. Remove the inner back panel EMI shield (refer to Figure 7-8) by removing the four screws located near the middle of the panel.

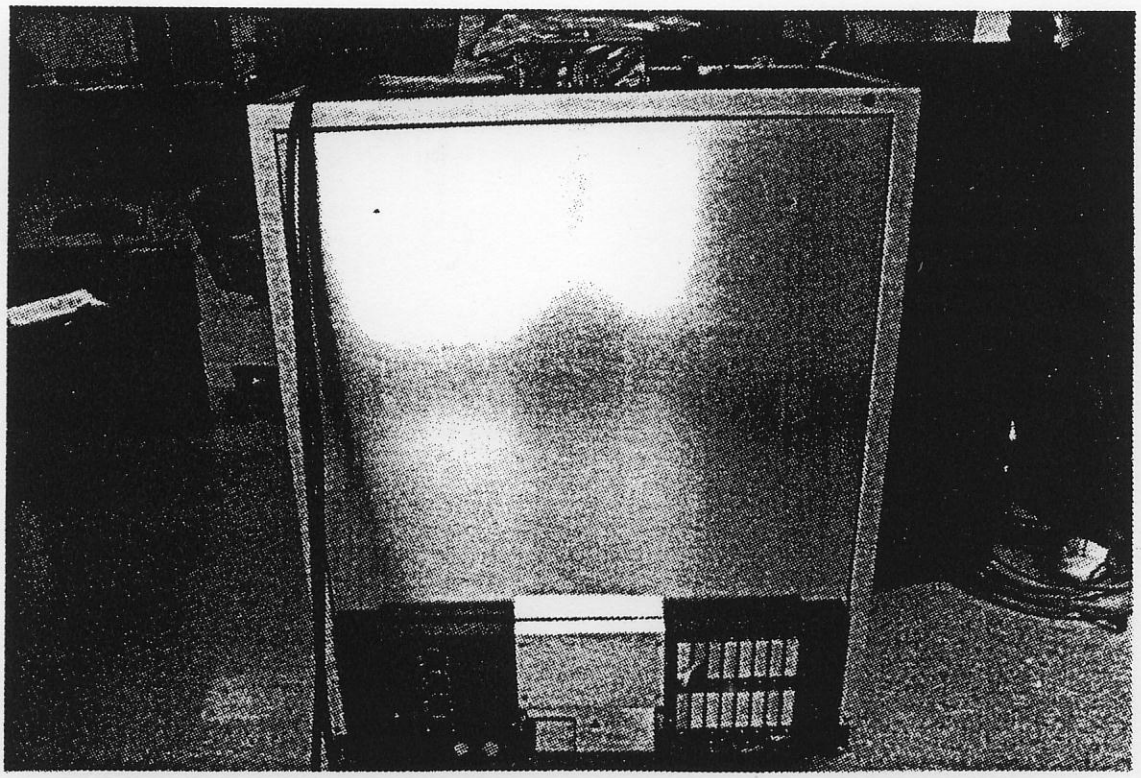


Figure 7-8. Inner Back Panel EMI Shield

FRP8

Replacing the Back Panel Assembly

Procedure

1. Replace the inner back panel EMI shield (Figure 7-8) by placing the panel back into the frame and securing the four panel screws.
2. Hang the panel on the panel mounting screw carefully. Refer to Figure 7-5.
3. Push the bottom of the panel into the frame; you should hear a click as the panel locks into position.

FRP9

Removing the IOS VME Boards

The VME IOS boards are the controllers for the individual peripherals. If a peripheral seems to be faulty, consider also that the controller may be failing. A photograph of the IOS VME boards is shown in Figure 7-9.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the IOS VME subsystem by depressing the DC inhibit/enable button on the small computer system interface (SCSI) assembly.

2. Label and remove the front ribbon cables from each IOS board. Refer again to Figure 7-9.

3. Loosen the retaining screws on the top and bottom of the board.

4. Grasp the board by the ejector handles located on the top and bottom of the board; push the top ejector handle up and the bottom ejector handle down at the same time and pull the board outward away from the backplane.

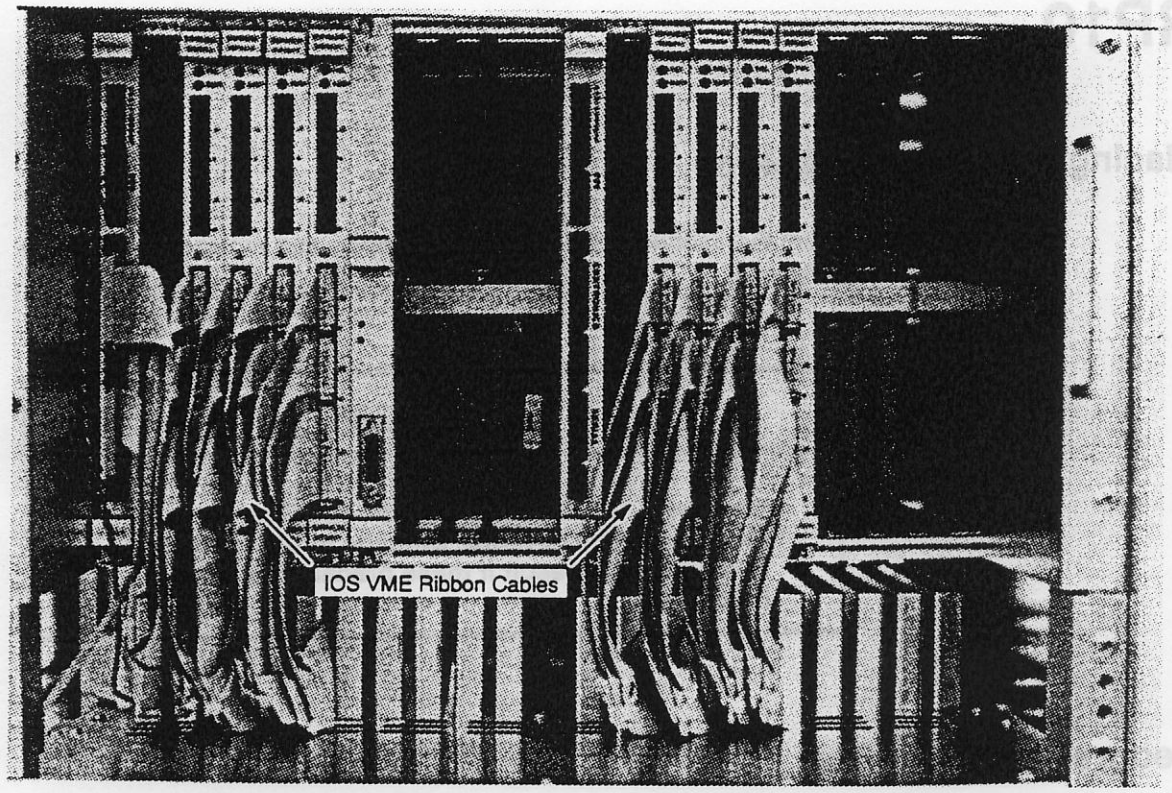


Figure 7-9. IOS VME Boards

FRP10

Replacing the IOS VME Boards

Ensure that individual board address jumpers and switches are properly configured.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Slide the IOS VME board into the correct slot along the glides until it comes in contact with the backplane.
2. Press the top and bottom of the board towards the backplane to set the board into the backplane connector.
3. Tighten the retaining screws.
4. Reconnect the ribbon cables.

FRP11

Removing the IOS VME Card Cage

The IOS VME card cage will have to be replaced if it has been determined that the backplane is faulty. None of the VME IOS boards will operate if the backplane is faulty.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Open the right side panel using FRP5.
3. Remove the back panel assembly using FRP7. If you have a multiple-cabinet system, you will have to separate the cabinets first. Refer to FRP48.
4. Remove the screws securing the card cage. Refer to Figure 7-10.
5. Ensure that all of the cables are properly labeled, and then disconnect the cables. Lay the cables flat so the card cage will not damage them.
6. Pull the card cage out as far as it will extend (the drawer has locks as shown in Figure 7-10), and then remove the entire maintenance small computer system interface (SCSI) as directed in the following steps.
7. Remove the DC inhibit/enable button cover on the VME card cage to access the inner screws. Refer to Figure 7-11 while performing the next three substeps.

    a. Remove the two securing screws on the left side of the EXABYTE-2 (EX-2) helical scan cartridge drive.

b. Remove the two securing screws that secure the hard disk drive to the SCSI. Retain the data cables.

c. Remove the two securing screws to release the streaming tape drive. Retain the data cables.

Ensure that the abovementioned components are placed in a static-safe area. Retain the SCSI cable.

8. Remove the six securing screws that cover the voltage buses in the vertical wireway. You may now remove the back bulk converter connector cover (Figure 7-12). This provides access to the card cage power plugs and the cable carrier.

9. Perform a voltage check on the system using FRP50.

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

10. Disconnect the power plug, power sense cable plug, and cable carrier (two screws) as shown in Figure 7-14.

NOTE: If your system contains tape drives, the interface cables will also be tied to the cable carrier. Disconnect these cables from the rear of the card cage and retain them.

11. Release the card cage locks and pull the card cage completely out. Refer to Figure 7-10.

CAUTION

The card cage has heavy weight concentration towards the back of the card cage. Exercise caution so that it does not drop and damage the card cage or cause injury.

12. Remove the VME boards from the old chassis one at a time and insert them into the new chassis in the correct locations.

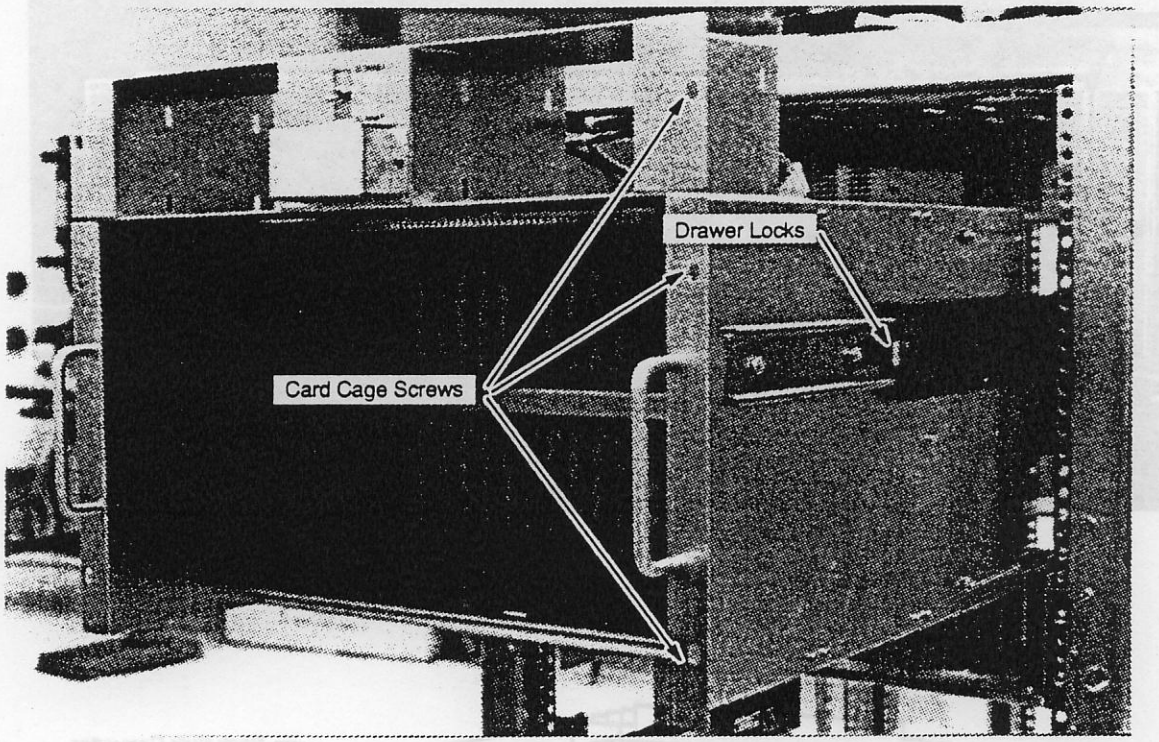


Figure 7-10. IOS VME Card Cage

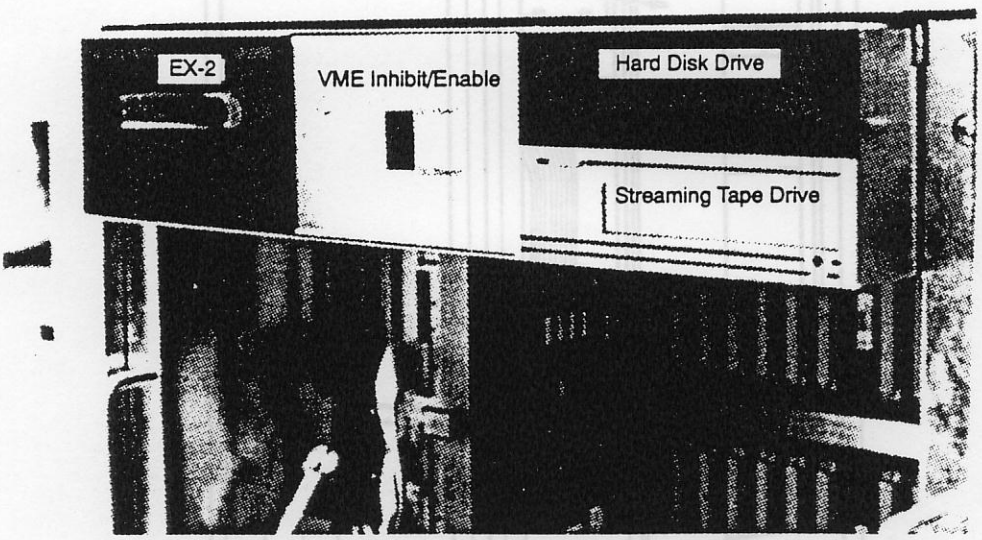


Figure 7-11. SCSI EX-2, Hard Drive, and Streaming Tape Drive

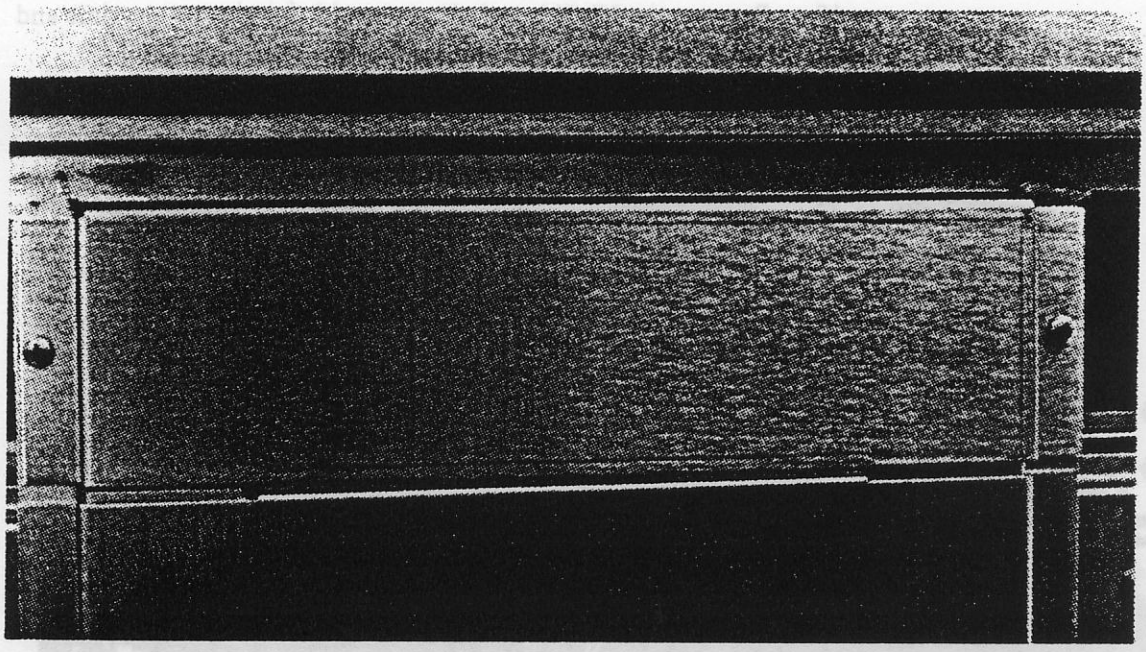


Figure 7-12. Back Bulk Converter Connector Cover

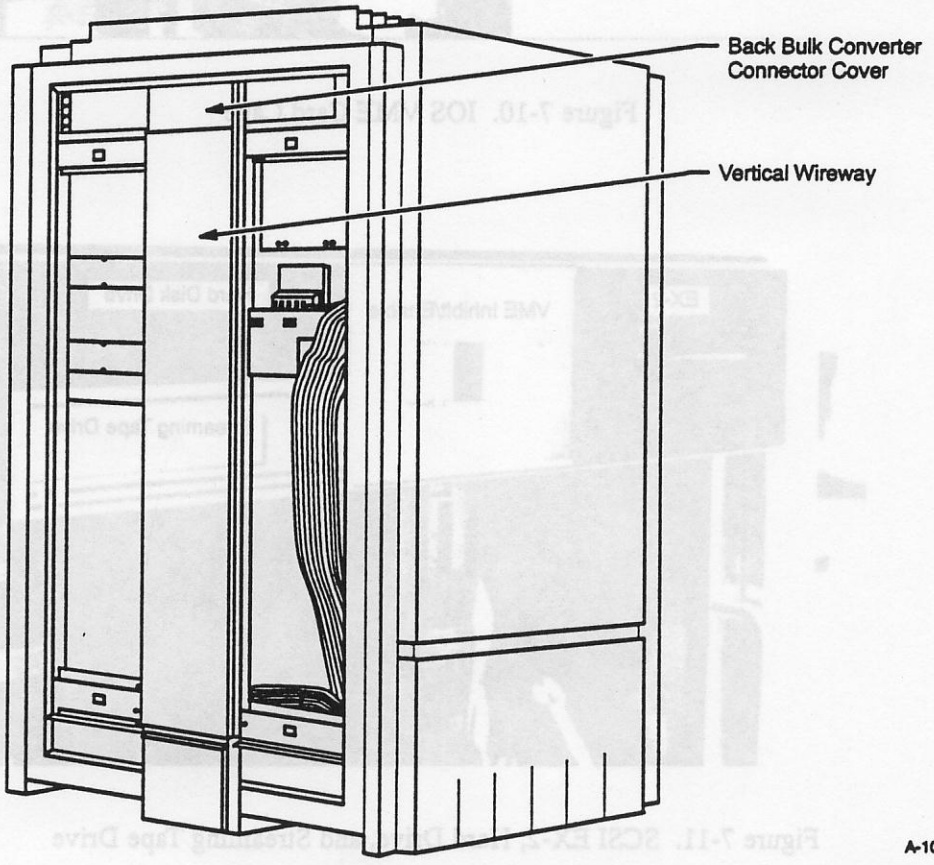


Figure 7-13. Vertical Wireway

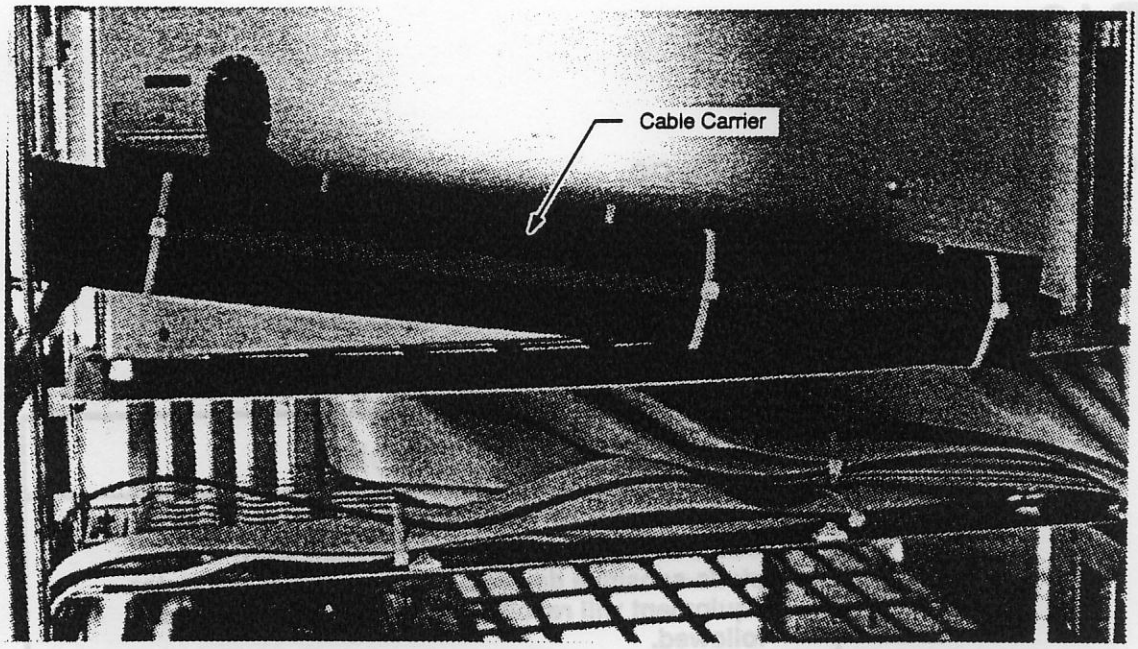


Figure 7-14. Cable Carrier

FRP12

Replacing the IOS VME Card Cage

Exercise caution when you reinstall the IOS VME card cage to ensure that no cables are damaged. Also ensure that the cables, when reinstalled, are seated properly into their connectors.

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Push the card cage back into the frame. If you have not moved each VME board and jumpers from the old card cage to the new card cage, do so at this time.
2. Reconnect the power plugs and cable carrier.
3. Replace the vertical wireway and back bulk converter connector cover by reinstalling all screws.
4. Replace the helical scan, and hard disk and streaming tape drive by replacing the screws that were removed in FRP11 Step 7.
5. Replace the four screws that secure the VME card cage to the 19-inch rack.
6. Replace the back panel and inner back panel EMI shield using FRP8.
7. Close the right side panel.
8. Power up the system using FRP1.

FRP13

Removing the IOS VME Power Supply

If you determine that an IOS VME power supply is faulty, use the following procedure to replace the power supply. The power supply is located behind the VME backplane.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Remove all cables.
3. Slide the IOS VME card cage out gently. Refer to FRP11 Steps 2 through 5.
4. Ensure that system voltage is at 0 using FRP50.

CAUTION

Lay the cables flat so you will not damage them as you are pulling out the IOS VME card cage.

5. Loosen, but do not remove, the four nuts (two on each side) that secure the power supplies. Refer to Figure 7-15.
6. Slide out the power supply assembly as far as it goes from the back of the card cage.

7. Remove the power supply guard by removing the two kep nuts on the top and the two screws on the bottom.

8. Disconnect all wiring and cables from the power supply. This includes removing two plugs, two large nuts on the bus bar, and three wires on the terminal block.

9. Disconnect and remove the securing screws on the back of the VME card cage while supporting the power supply, and pull it out.

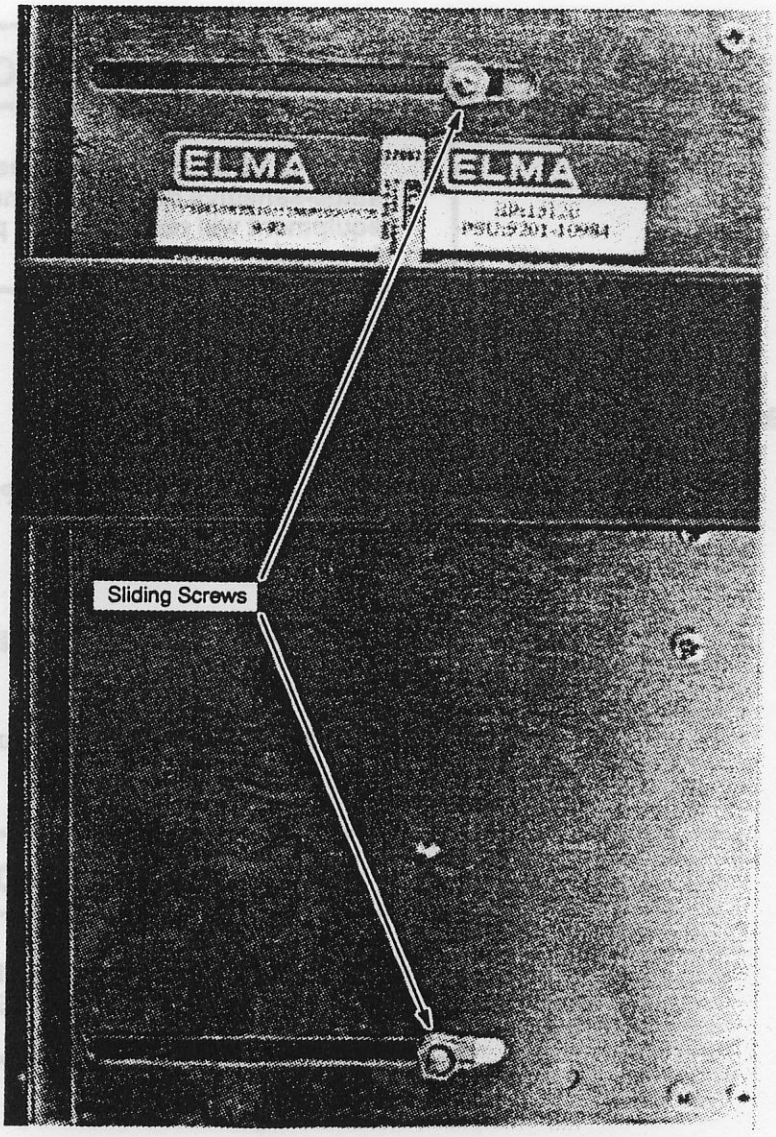


Figure 7-15. VME Power Supply Drawer

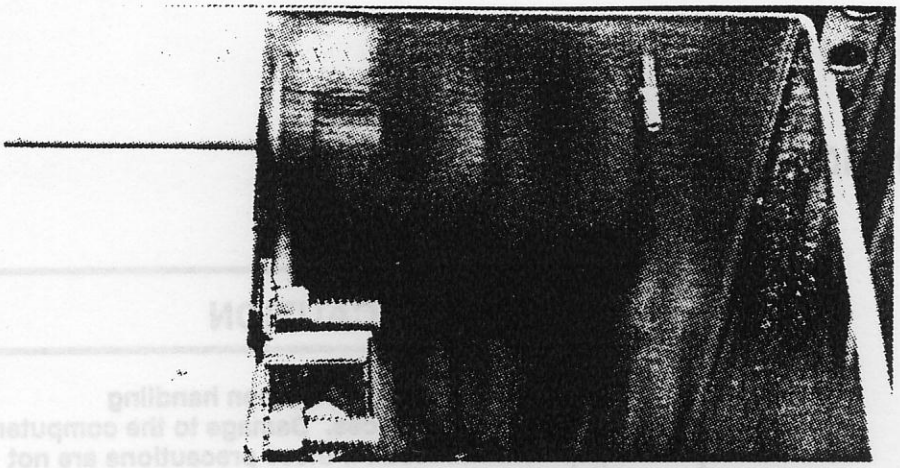
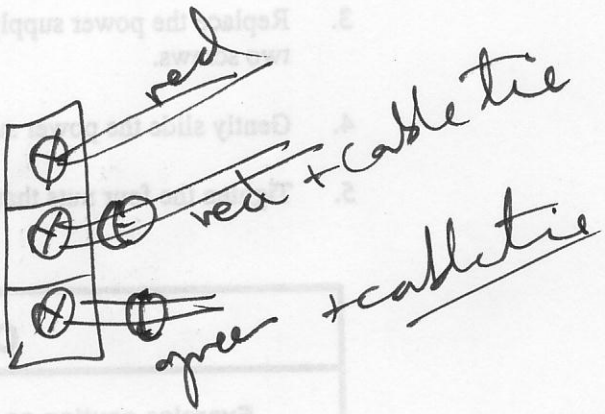


Figure 7-16. VME Power Supply



FRP14

Replacing the IOS VME Power Supply

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Insert the new power supply and replace the securing screws.
2. Reconnect all wiring and cables to the power supply.
3. Replace the power supply guard by replacing the two kep nuts and two screws.
4. Gently slide the power supply into place on the card cage.
5. Tighten the four nuts that secure the power supply.

CAUTION

Exercise caution so you do not damage the cables as you are pushing in the IOS VME card cage.

6. Slide the IOS VME card cage back into the frame gently.
7. Replace the four screws on the card cage.
8. Replace the cables on VME boards.
9. Reseat the IOS VME board cables.
10. Power up the system using FRP1.

FRP15

Removing the CPU and Memory Boards

Use proper ESD procedures when handling mainframe boards (refer to "ESD Precautions" at the beginning of this section). When you find, by using diagnostics, that a CPU or memory board is faulty, use the following procedure to remove the board.

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedures

1. Power off the CPU and memory by depressing the respective DC enable/inhibit buttons. Refer to Figure 7-17.
2. Remove the ribbon cables from the boards.
3. Remove the module lock bar by removing its retaining screw.
4. Remove the Y1 cables from the CPU boards.
5. Grasp the two extraction levers on the front top and bottom of the appropriate board; pull out and push up on the upper lever while you pull out and push down on the lower lever. Refer to Figure 7-18.
6. Slide the board carefully out of the card cage, ensuring that no cables are damaged.
7. Place the defective board in an ESD-safe bag.

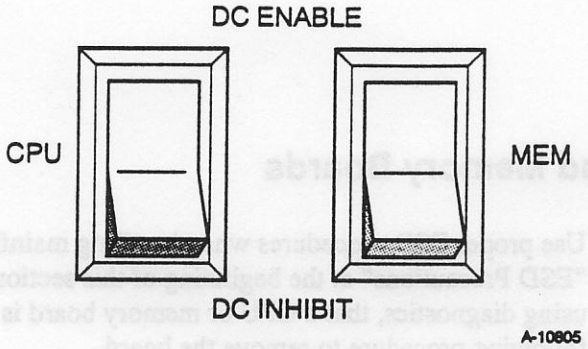


Figure 7-17. CPU and Memory DC Enable/Inhibit Buttons

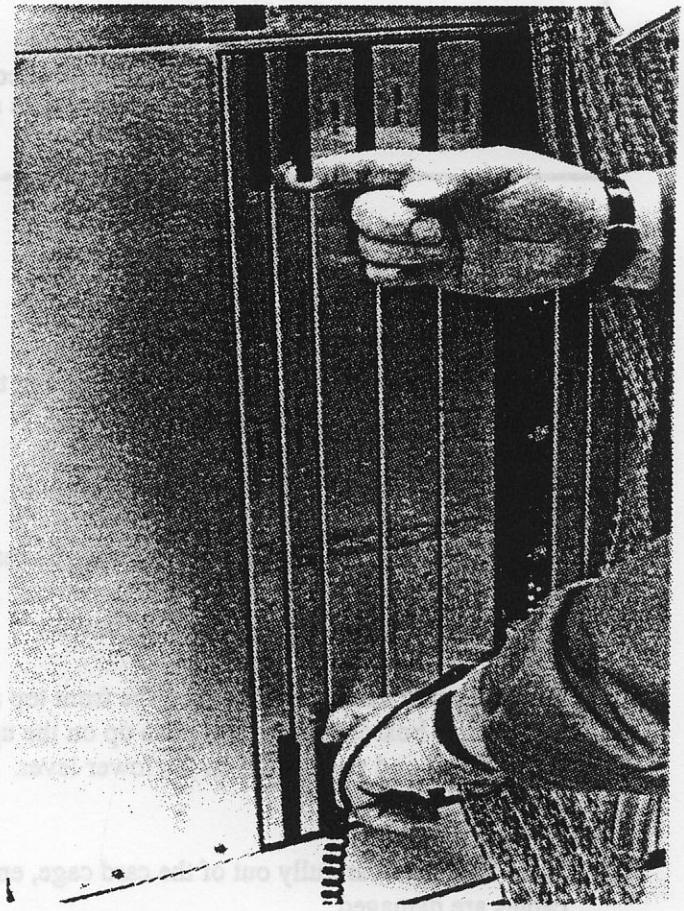


Figure 7-18. Removing CPU Board

FRP16

Replacing the CPU and Memory Boards

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Remove the replacement board from the ESD-safe bag or shipping container.
2. Spray the back panel connector pins with a degreaser spray.
3. Slide the board into the appropriate slot. Note that the logic chips should be on the right side of the board, if it is positioned correctly.
4. Push the board, using the extraction lever, along the front edge to seat it in the backplane connector.
5. Reconnect the ribbon cables to the CPU boards.
6. Replace the module lock bar.
7. Power on the CPU assembly by pressing the CPU and memory DC enable/inhibit buttons.

FRP17

Removing the Clock Module

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the CPU and memory by pressing the DC enable/inhibit button.
2. Open the right side panel door.
3. Remove the ten screws on the CPU card cage and pull it out.
4. Remove the frequency cable by unscrewing the lower nut on the frequency cable connector. Refer to Figure 7-19.
5. Loosen the two retaining screws.
6. Pull out the CPU clock module.

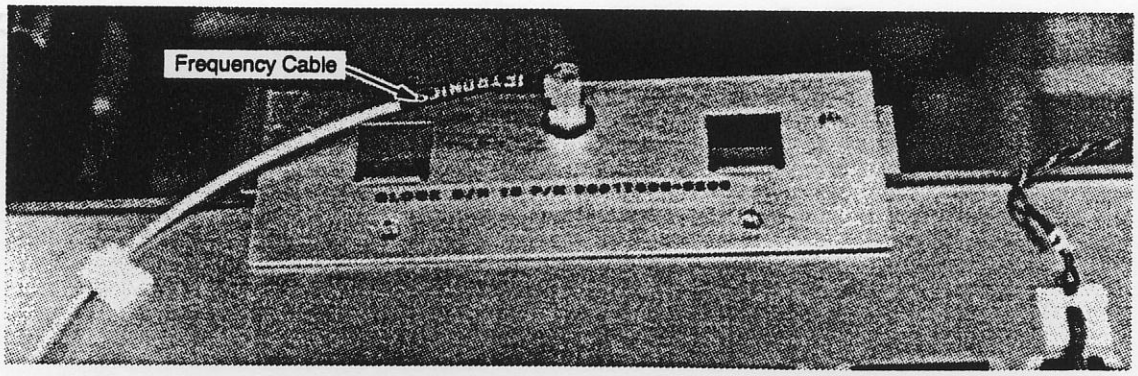


Figure 7-19. Clock Module Frequency Cable

FRP18

Replacing the Clock Module

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Insert the new clock module.
2. Replace the frequency cable.
3. Spray connectors with degreaser.
4. Tighten the two retaining screws.
5. Ensure that the module is seated properly.
6. Push CPU card cage in and reinstall screws.
7. Restore power to the CPU and memory by depressing the DC enable/inhibit button.

FRP19

Removing the CPU Card Cage

The CPU card cage will have to be removed and replaced if the CPU backplane is faulty.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Open the right side panel.
3. Disconnect all CPU and memory board cables.
4. Remove all CPU and memory boards and place them in an ESD-protected container. Refer to FRP15 to remove these boards.
5. Remove the ten screws on the CPU card cage. Refer to Figure 7-20.
6. Remove the filter in the lower fan tray. Refer to Figure 7-20.
7. Remove the lower fan tray in the bottom of the CPU card cage as shown in Figure 7-20.
8. Remove the back panel and inner back panel EMI shield to gain access to the card cage power plugs and the vertical wireway cover. Refer to FRP7.
9. Extend the card cage from the front of the CPU using the grasp handles.
10. Remove the four screws retaining the wireway cable carrier bracket. Refer to Figure 7-21.

11. Label and then unplug the six power and sense cables.

12. Label and remove both power supplies. Refer to FRP21.

13. Remove the clock module using FRP18, Steps 3 and 4.

14. Drop the cables inside the chassis to prevent damage when removing.

15. Release the card cage locks and pull the card cage completely out of the chassis.

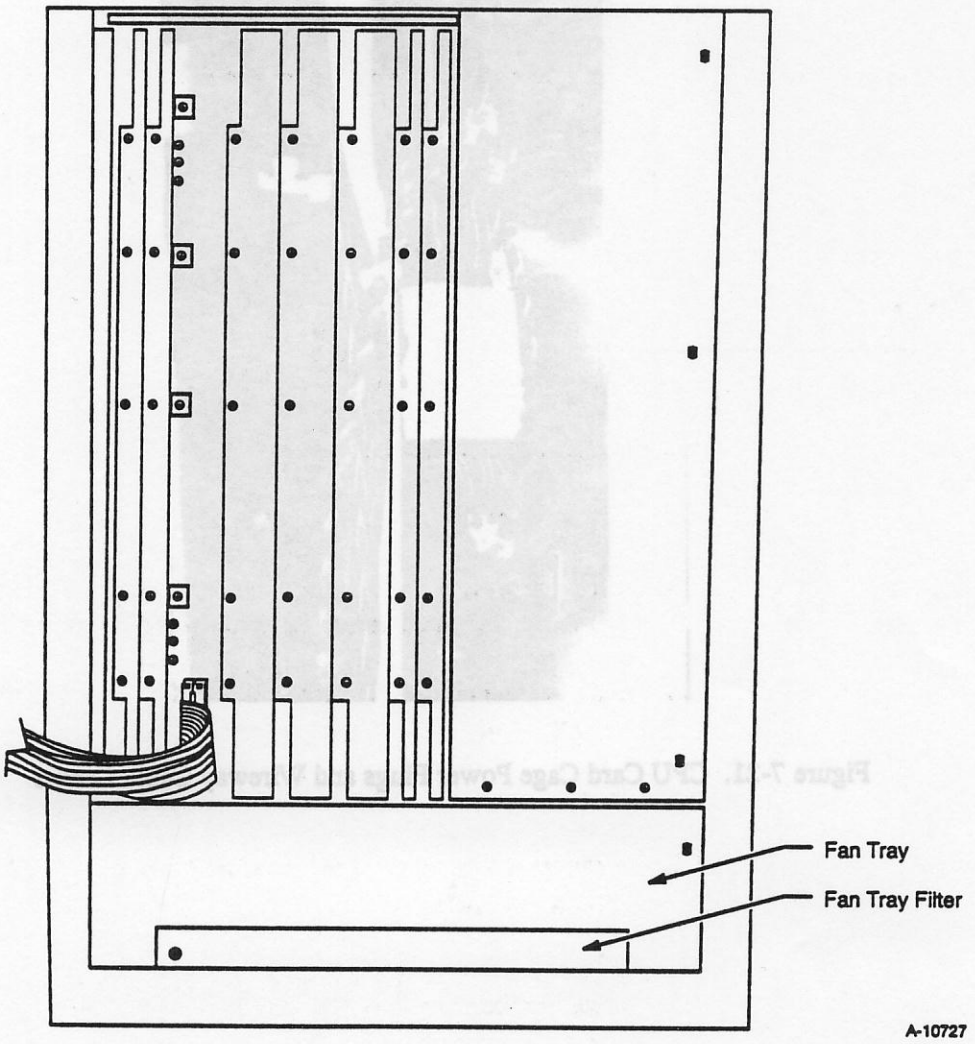


Figure 7-20. CPU Card Cage

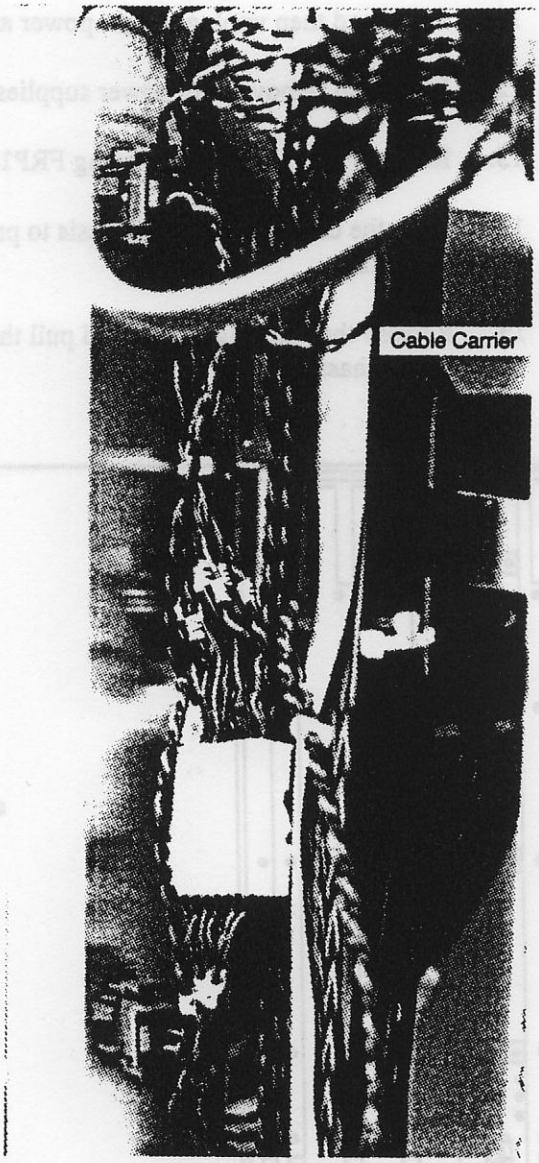


Figure 7-21. CPU Card Cage Power Plugs and Wireway Cable Carrier

FRP20

Replacing the CPU Card Cage

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Push the new CPU card cage onto the drawer rails. Leave the card cage extended out of the chassis.
2. Reconnect the power plugs and cable carrier to the lower fan tray.
3. Replace the lower fan tray into the chassis.
4. Replace the filter in the lower fan tray.
5. Reinstall the clock module using FRP17 Steps 2 and 3.
6. Replace the two power supplies. Refer to FRP22.
7. Push the CPU card cage back into the system.
8. Replace the ten screws securing the CPU card cage.
9. Reinstall the CPU and memory boards using FRP16.
10. Reconnect the ribbon cables to the CPU boards.
11. Replace the vertical wireway cover.
12. Replace the inner back panel EMI shield.
13. Power up the system using FRP1.

FRP21

Removing the CPU and Memory Power Supply

The CPU power supplies are the sole source of power to the CPU. Use the following procedure if you suspect that a power supply is faulty.

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Open the right panel using FRP5.
3. Remove the ten screws on the CPU card cage.
4. Pull out the card cage until it is fully extended.
5. Verify that the voltage bus reading is at 0 volts by using FRP50.
6. Loosen the two screws that secure the power supply to the frame at the top of the power supply. Refer to Figure 7-22.
7. Remove the two screws from the output power buses on the bottom of the power supply.

8. Grasp the power supply handle and carefully pull up from the card cage. Refer to Figure 7-22.

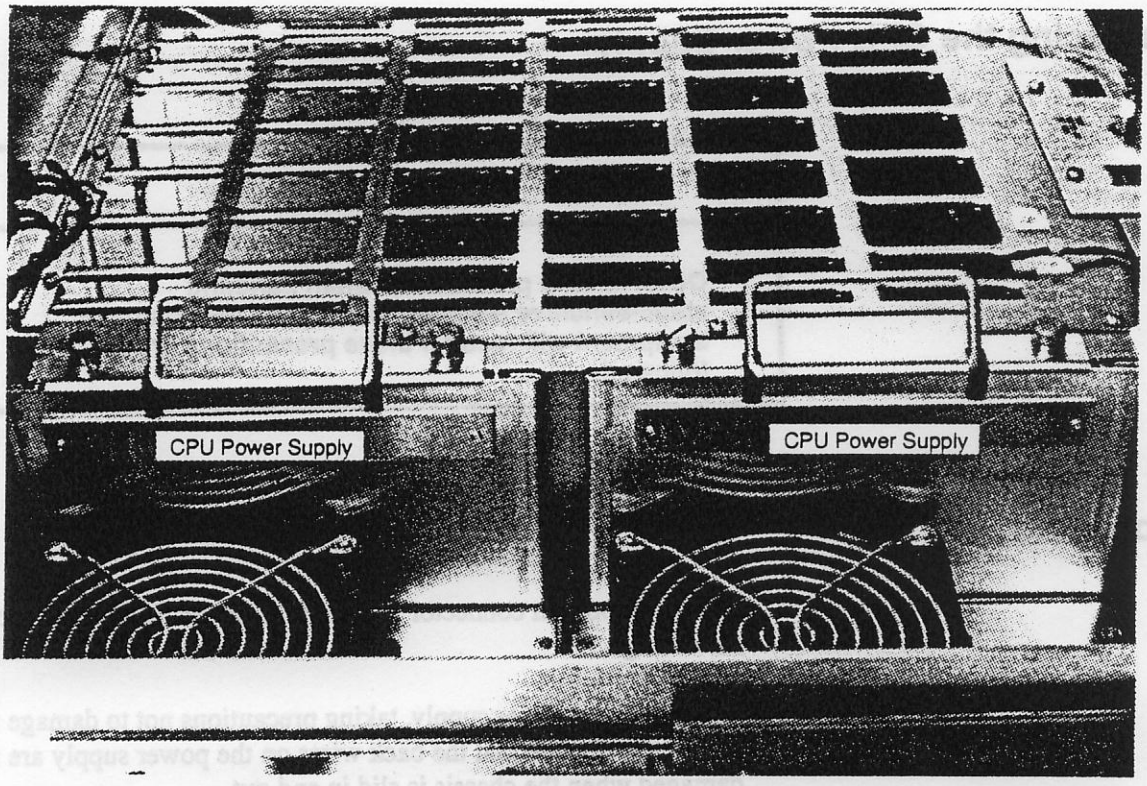


Figure 7-22. CPU Power Supplies - Top View

FRP22

Replacing the CPU Power Supply

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Check the bottom connector and the pins on the new power supply for damage.
2. Insert the new power supply, taking precautions not to damage the connector. Ensure that the back wires on the power supply are not damaged when the chassis is slid in and out.
3. Replace the two screws that secure the power supply to the mainframe.
4. Replace the two allen screws that secure the power supply to the buses.
5. Grasp the card cage handles and carefully push the card cage back into the chassis.
6. Replace the ten card cage screws.
7. Close and replace the right side panel using FRP6.
8. Power up the system using FRP1.
9. Verify power supply operation by ensuring that the fans are working.

FRP23

Removing the Bulk Converter

The bulk converter is a self-contained unit that houses four power supplies: two 12-V power supplies to operate the fans and two 380-V power supplies to provide primary DC power. If any one of these power supplies becomes defective, it is necessary to replace the entire bulk converter.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Remove the front panel and inner front panel EMI shield using FRP3.
3. Remove the back panel and inner back panel EMI shield using FRP7.
4. Remove the top grill panels (slotted trim) by removing the two flathead screws on the top of the chassis next to the side panels. The top grill panel then lifts off by sliding on two guide pins on the bulk converter. Refer to Figure 7-33 for a photograph of the top fan tray perforated cover.

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

5. Remove the front inner voltage access panel by removing six screws (three on each side) while supporting the weight of the control assembly at the same time. Refer to FRP29. Support the control panel as you lower it to the floor and rest it against the cabinet. Take precautions to avoid damage to the cable harnesses and connectors.

6. Remove the front and back bulk converter access plates by removing the two screws from each plate. Refer again to Figure 7-12.

7. Disconnect the bulkhead connectors (six on the front and five on the back) from the bulk converter. Refer to Figure 7-23.

8. Remove the left and right fan top fan tray perforated covers by removing four screws from each assembly. Use caution; these edges may be sharp.

9. Remove the fan tray screws, which are four Phillips screws and four hex screws.

10. Lift the left side fan tray and slide the trays about 4 in. until they are clear of the bulk converter. Do not strain or damage the fan tray wire harness.

11. Remove the four bulk converter mounting screws after the top fan tray perforated covers have been removed. Refer to Figure 7-24.

12. Extend the upper peripheral trays and/or the IOS card cage about 4 in., enough to enable hand holds on the bulk converter. The IOS board cables do not have to be removed.

CAUTION

To avoid personal injury and machine damage, use two people to lift the bulk converter; it is very heavy. Take care not to damage the connectors.

13. Lift the bulk converter straight up until these connectors contact the frame. Move the bulk converter forward or backward to allow clearance of one of the connectors. Tip the bulk converter up on the end that is clear and lift it from the chassis.

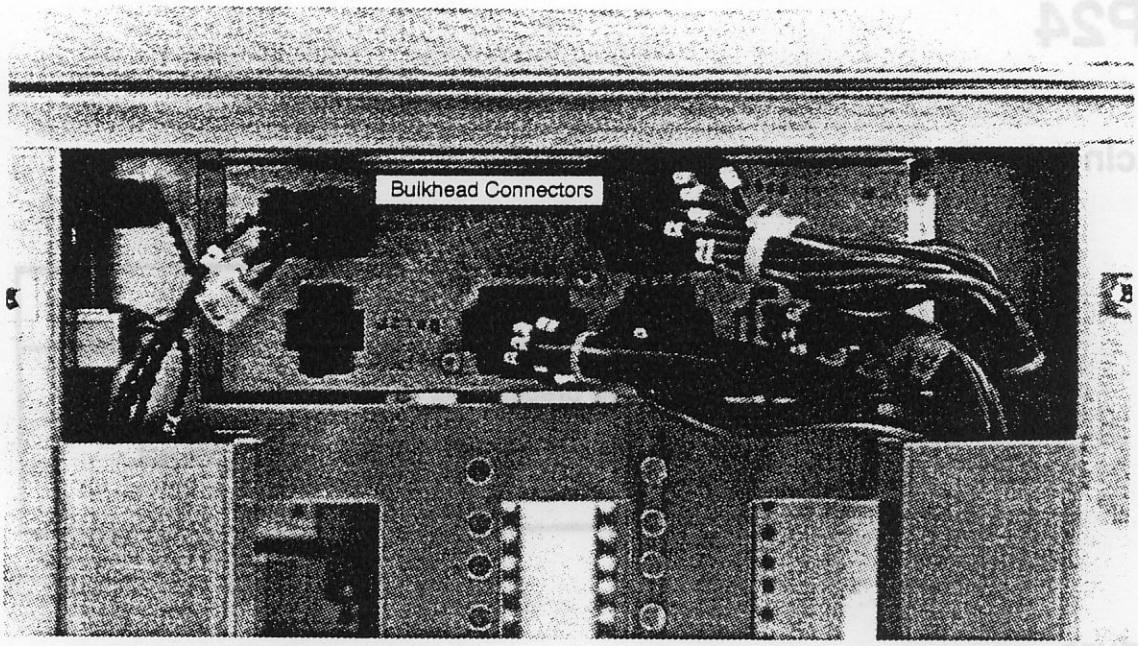


Figure 7-23. Bulkhead Connectors

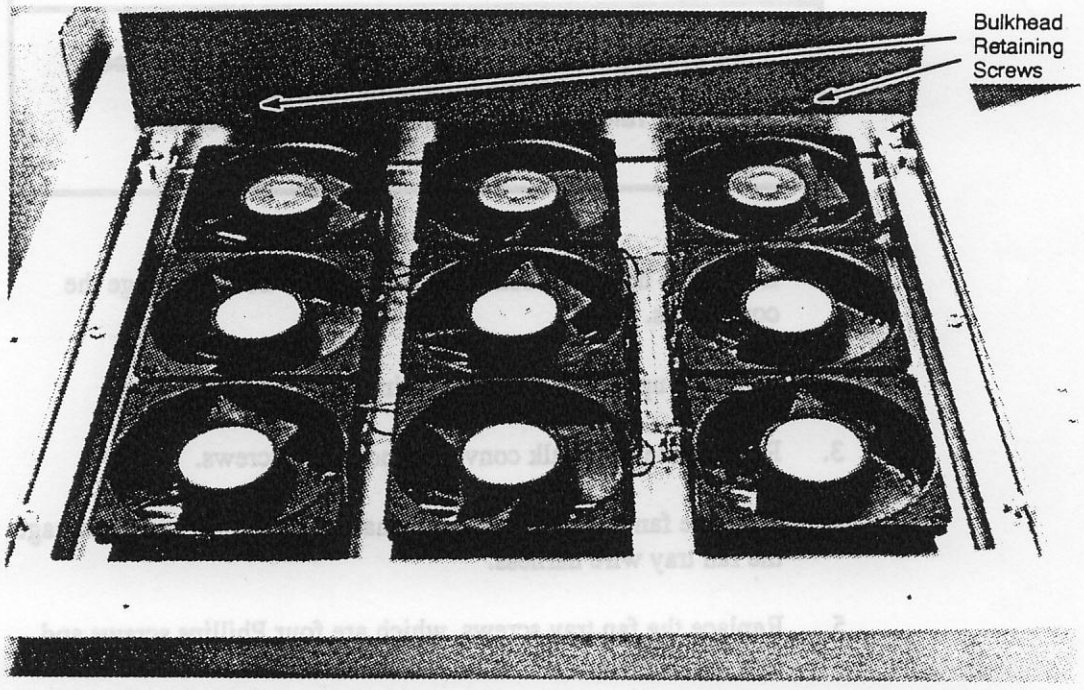


Figure 7-24. Bulkhead Retaining Screws

FRP24

Replacing the Bulk Converter

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

CAUTION

To avoid personal injury and machine damage, use two people to lift the bulk converter; it is very heavy. Take care not to damage the connectors.

1. Lower the new bulk converter, taking care not to damage the connectors.
2. Place the upper peripheral trays in their original positions.
3. Replace the four bulk converter mounting screws.
4. Slide the fan trays back into the chassis. Do not strain or damage the fan tray wire harness.
5. Replace the fan tray screws, which are four Phillips screws and four hex screws.
6. Replace the left and right top fan tray perforated covers.
7. Reconnect the bulkhead connectors (six on the front and five on the back) to the bulk converter.

8. Replace the front and back bulk converter connector covers by replacing the two screws on each plate.

9. Replace the control assembly and panel by replacing the six screws (three on each side) on the mounting panel. Support the weight of the control assembly as you lift it and place it back in the bulk converter location.

10. Replace the back panel and inner back panel EMI shield using FRP8.

11. Replace the front panel and inner front panel EMI shield using FRP4.

12. Power up the system using FRP1.

FRP25

Removing the Capacitor Bank

The capacitor bank maintains power to the system in the event that momentary power line failures occur.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

1. Power down the system using FRP2.
2. Unplug the system from the power source.
3. Remove the front and back panels and the inner panel EMI shields using FRP3 and FRP7 respectively.
4. Remove the inner voltage access panel (six screws) from the rear of the system.
5. Verify that the high-voltage bus is discharged to 0 volts by using FRP48.

6. Remove the capacitor bank connector access plates. The front plate is a panel with two screws (Figure 7-6), and the back plate is a box with four screws. Refer to Figure 7-25.

7. Disconnect the connectors from the front and back of the capacitor bank. Refer to Figure 7-26.

8. If you are repairing the mainframe cabinet remove the incoming power module using FRP27 Steps 5 and 6. Set the incoming power module to one side.

    a. If you are repairing the mainframe cabinet, remove the four mounting screws in the incoming data cable module and set it off to the side. The cables remain attached.

9. Remove the AC input-cable-strain-relief-plate (three screws) from the lower left corner of the back of the capacitor bank. Refer to Figure 7-25.

    a. Remove the two outer screws.

    b. Loosen the screw located toward the back of the relief plate.

10. Label, then disconnect, the incoming power from the capacitor bank.

11. Remove the two screws from the front upper corners of the capacitor bank on the front of the system. Keep these screws separate because they are different. The unit should slide freely to the rear. Use caution, as the capacitor bank is very heavy.

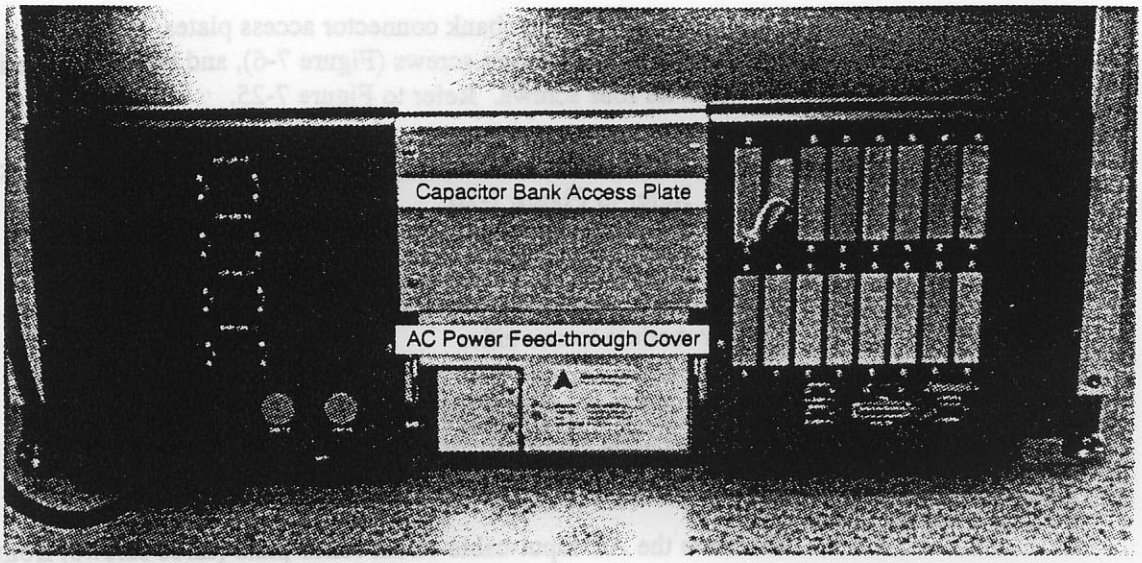


Figure 7-25. Back Capacitor Bank Access Plate

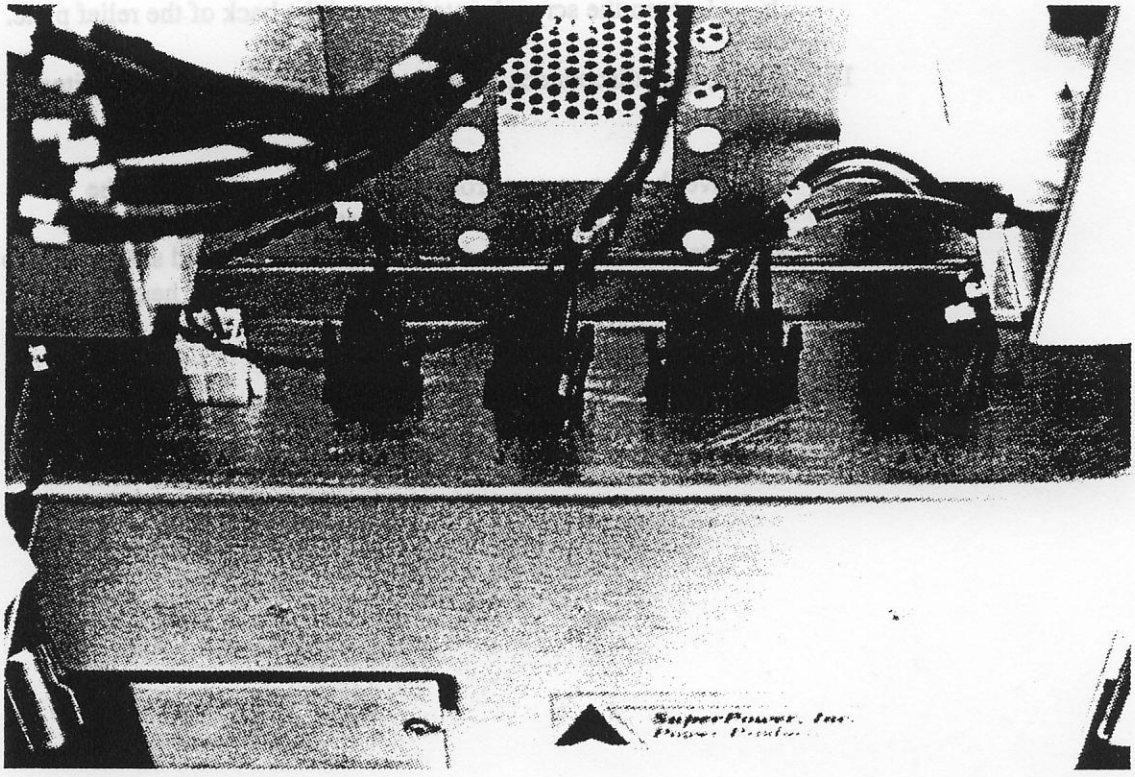


Figure 7-26. Capacitor Bank Connectors

FRP26

Replacing the Capacitor Bank

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

1. Check the incoming air filter to determine whether it needs cleaning or replacement.
2. Slide the replacement unit in from the rear, and then secure it from the front with the two screws.
3. Reconnect the AC input cable and cover the box and plugs in the front and rear.
4. Reconnect the connectors on the front and back of the capacitor bank.
5. Replace the capacitor bank access plates.
6. Verify that the capacitor bank is operational by using the following procedure.

    a. Place the DVM leads into the high-voltage socket.

b. Power off the system by depressing the emergency power-off (EPO) button.

c. Observe the voltage rapidly decline to around 16 V. The voltage drop will now progress slowly to 0 V.

7. Replace the front and back panels and the EMI shields using FRP4 and FRP8.

8. Power up the system using FRP1.

FRP27

Removing the Incoming Power Module

The incoming power module may be replaced if the circuit breaker is faulty or if the ON/OFF switches are inoperable.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

1. Power down the system using FRP2.
2. Unplug all AC cables from their power sources.
3. Remove the back panel and inner back EMI shield using FRP7. Use FRP50 to ensure that the system has completely powered down.
4. Remove the back bulk converter connector cover.
5. Remove the capacitor bank connector access plate (shown in Figure 7-25) from the upper right corner of the incoming power module (four screws).

6. Unplug the J2, J3, and J4 connectors from the incoming data cable module. Refer to Figure 7-27. J3 is attached with two screws.

7. Remove the two long and two short screws from the incoming power module.

8. Carefully lay the incoming power module with the breaker-side down beside the system.

9. Remove the incoming AC cable strain reliefs using suitable spanners, and remove the cables. Refer to Figure 7-28 for a photograph of the strain reliefs. The procedure for removing the strain reliefs can be found inside the incoming power module. Use a medium-sized flat-bladed screwdriver.

10. Remove the outgoing AC cables, using a pliers to remove the strain-relief devices. (Refer to Figure 7-28.) The cables should then pull out easily.

11. Thoroughly inspect all cables for damage. Damaged cables must be properly repaired or replaced.

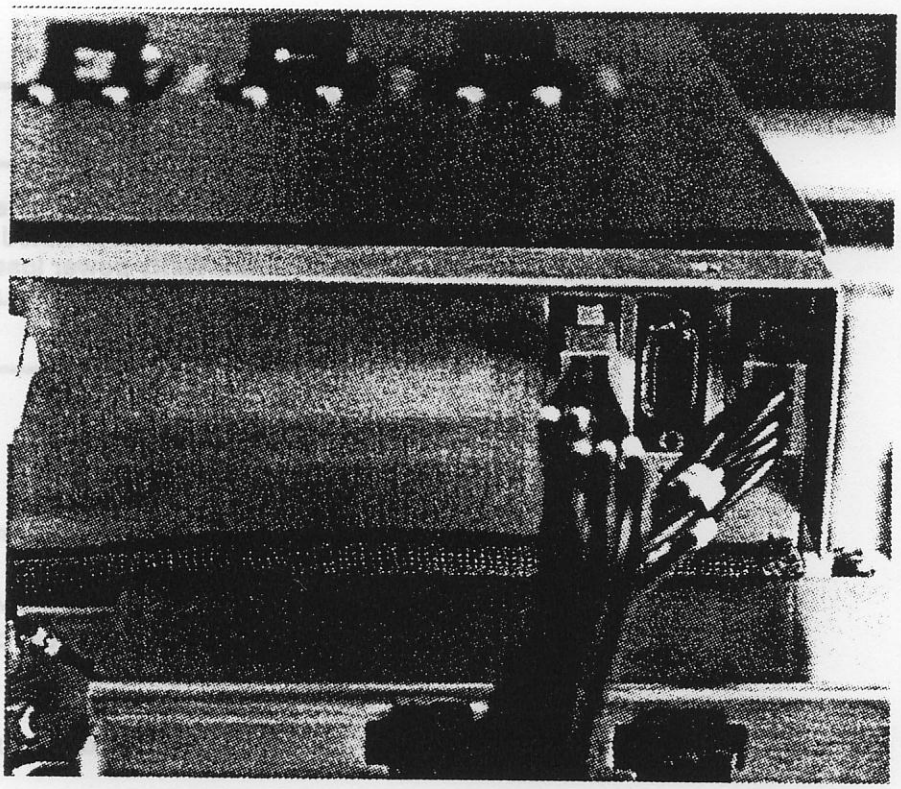


Figure 7-27. Incoming Power Module Connectors and Data Cable

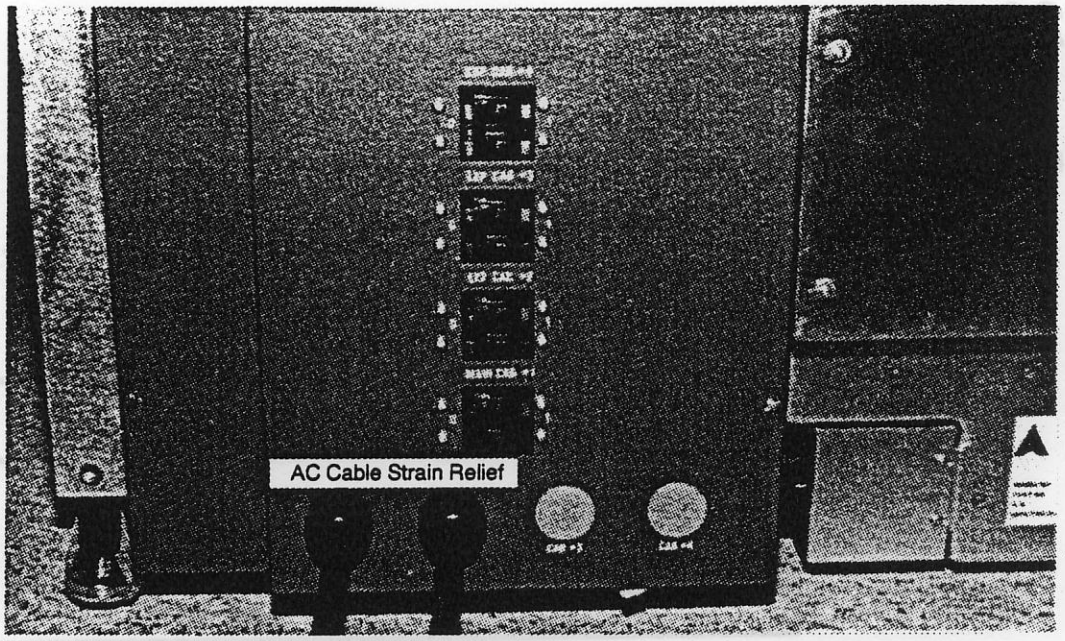


Figure 7-28. AC Cable Strain Relief

FRP28

Replacing the Incoming Power Module

The field repair practice will be to replace the entire incoming power module.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

1. Insert the new incoming power module.
2. Transfer the AC cables to the new incoming power module assembly and secure them with the strain relief devices.
3. Replace the back plate of the incoming power module assembly and secure it with ten countersunk screws.
4. Replace the two long and two short screws on the incoming power module.
5. Reconnect the J2, J3, and J4 connectors to the incoming power module.
6. Replace the capacitor bank connector access plate (four screws).

7. Replace the back bulk converter connector cover.

8. Replace the back panel and inner back panel EMI shield using FRP8.

9. Replug all AC power cables to their power source.

10. Power up the system using FRP1.

FRP29

Removing the Control Panel

The control panel (Figure 7-29) displays the status of the system. The field repair practice for the control panel is to remove and replace the entire assembly.

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Remove the front panel and inner front panel EMI shields using FRP3.
3. Remove the eight screws, four on each back side, from the control panel assembly. Hold on to the assembly as you remove the last screws, as it may fall. Refer to Figure 7-30.
4. Ensure that all the connectors are properly labeled, and then remove each of them to release the control panel. The following list describes the cables and connectors that you will remove.
   - Two ribbon cables
   - One smaller connector
   - Black wires from EPO button that run into the mainframe and plug in near the CPU card cage. Cut the two wire wraps and unplug it from the chassis.
5. The control panel is now removed.

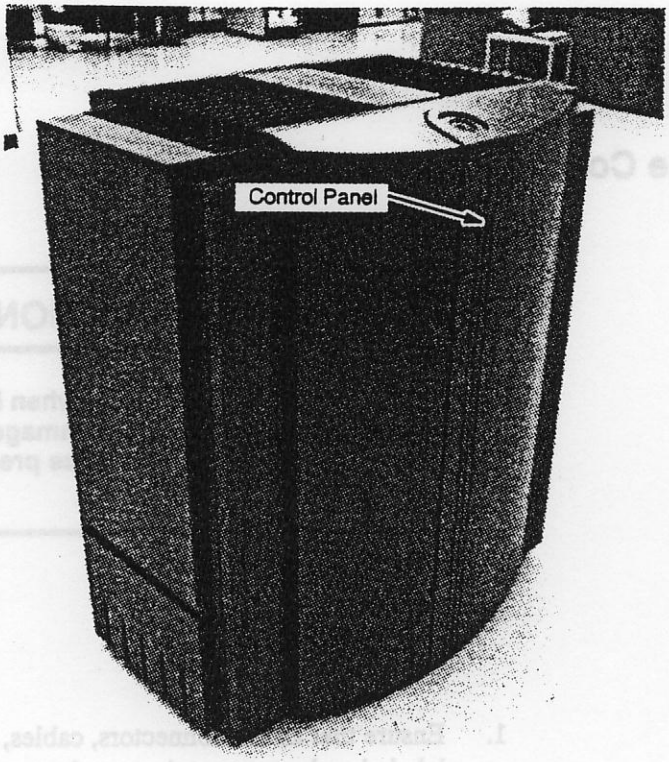


Figure 7-29. Control Panel

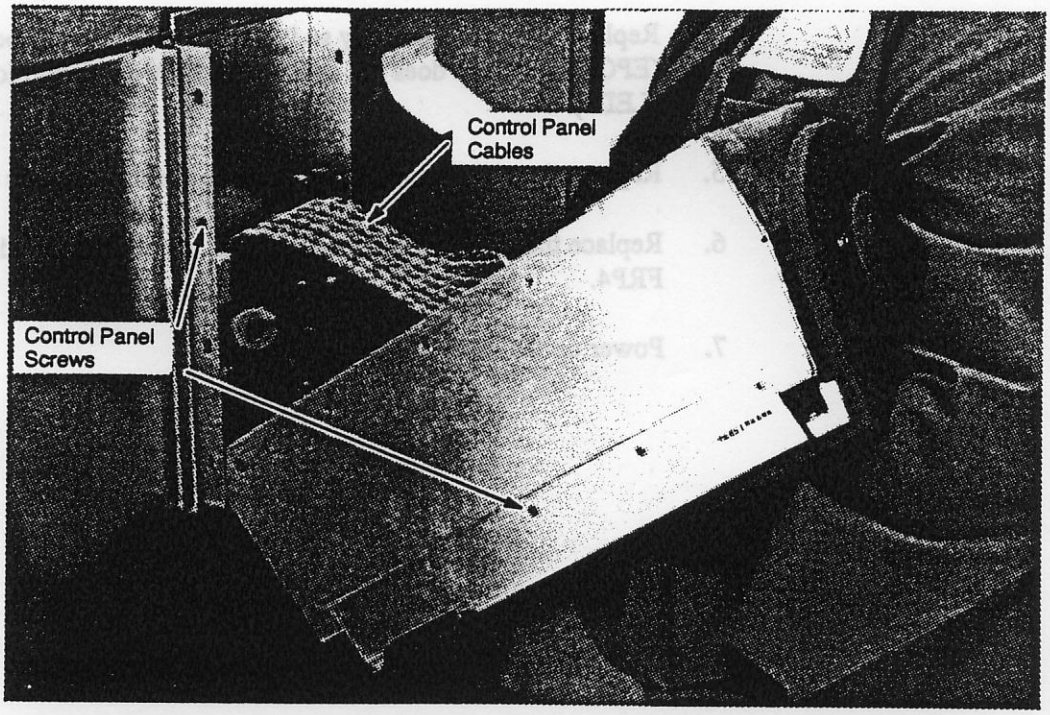


Figure 7-30. Control Panel Cables and Connectors

FRP30

Replacing the Control Panel

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Ensure that all the connectors, cables, and wires are properly labeled and reconnect them to the control board.
2. Ease the board back into the trim.
3. Replace the six screws on the control board.
4. Replace the cover carefully so it clears the emergency power-off (EPO) button and does not damage the light-emitting diodes (LEDs).
5. Replace the eight screws that attach the control board to the panel.
6. Replace the front panel and inner front panel EMI shield using FRP4.
7. Power up the system using FRP1.

FRP31

Removing the Lower Fan Tray

The status lights on the control panel illuminate when a fan is not operating and should be replaced. Refer to Figure 7-20 for a photograph of the lower CPU fan tray. Figure 7-31 is a photograph of the left lower fan tray.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Open the side panel using FRP5.
3. Remove the two securing screws on the fan tray. Refer to Figure 7-31.

NOTE: Only the right CPU cabinet has a tray that is mounted under the CPU card cage. It has a different cable-routing system. Extend this tray halfway and disconnect the plugs.

4. Pull out the filter. Refer to Figure 7-31.
5. Pull the fan tray out while supporting it, as it is not fixed to the sliders. If you are removing a lower fan tray under the CPU chassis, lift up slightly as you pull the tray out.
6. When the left lower fan tray is just clear of the frame rest, support the tray while you disconnect the power and sense plugs. Refer to Figure 7-32.
7. Remove the screw for the cable carrier. The cable ties may have to be clipped to allow cable removal. The tray should now be clear of the frame. Refer to Figure 7-32.

Figure 7-31. Left Lower Fan Tray

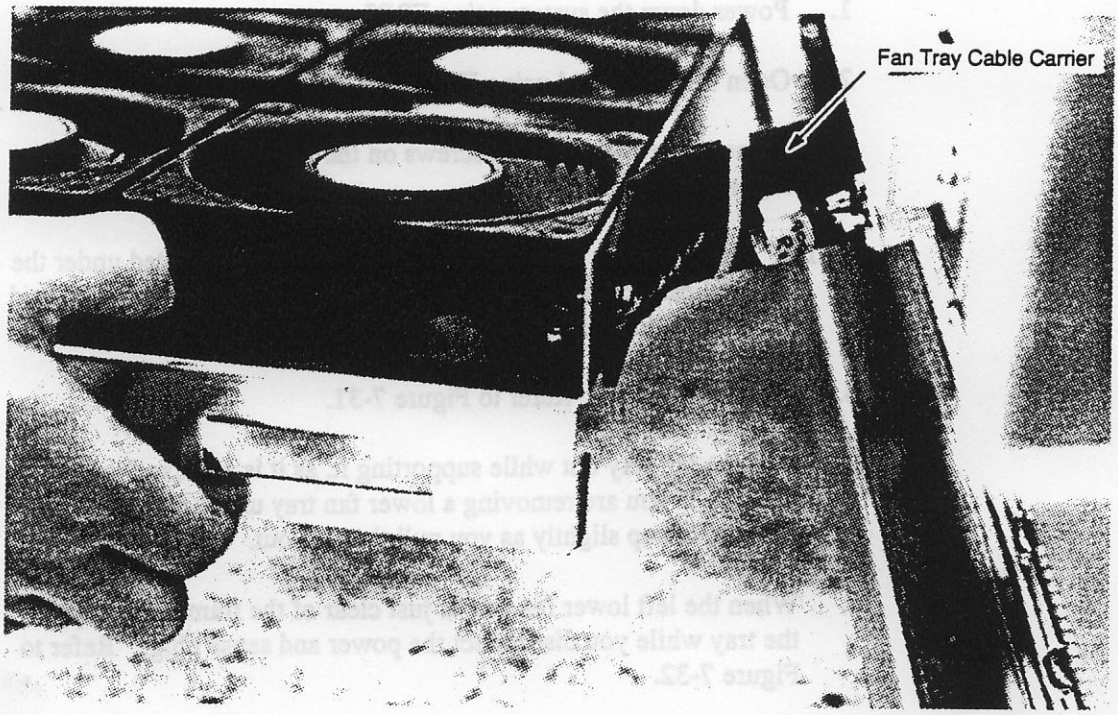


Figure 7-32. Lower Fan Tray Cable Carrier

FRP32

Replacing the Lower Fan Tray

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Replace the screw for the cable carrier on the replacement fan tray. If the cable ties have been clipped, reconnect them.
2. Push the tray in several inches, then reconnect the power and sense plugs. The tray is not fixed to sliders, so you will have to support it.
3. Push the fan tray all the way back in.
4. Replace the two securing screws.
5. Close the side panel.
6. Power up the system using FRP1.

FRP33

Removing the Upper Fan Tray

The control panel status lights indicate when a fan is not operating and must be replaced.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. To remove the right upper fan tray, remove the front panel and inner front panel EMI shield (FRP3). To remove the left upper fan tray, remove the back panel and inner back panel EMI shield (FRP7).
3. Remove the two countersunk screws securing the top grill panel on the top of the chassis next to the side panels. Refer to Figure 7-33.
4. Slide the panel to the side on its guide pins and then lift it out.
5. Remove the four screws from the top fan tray perforated cover and lift the cover out. The perforated cover may have sharp edges.
6. Remove the four Phillips screws and four hex screws from the fan tray.
7. Disconnect the fan power plug and warning signal plug located in the bulk converter panel area (P5 power left and right, P8 warning left, and P7 warning right). Refer to Figure 7-34.
8. Lift the fan tray clear of the chassis.

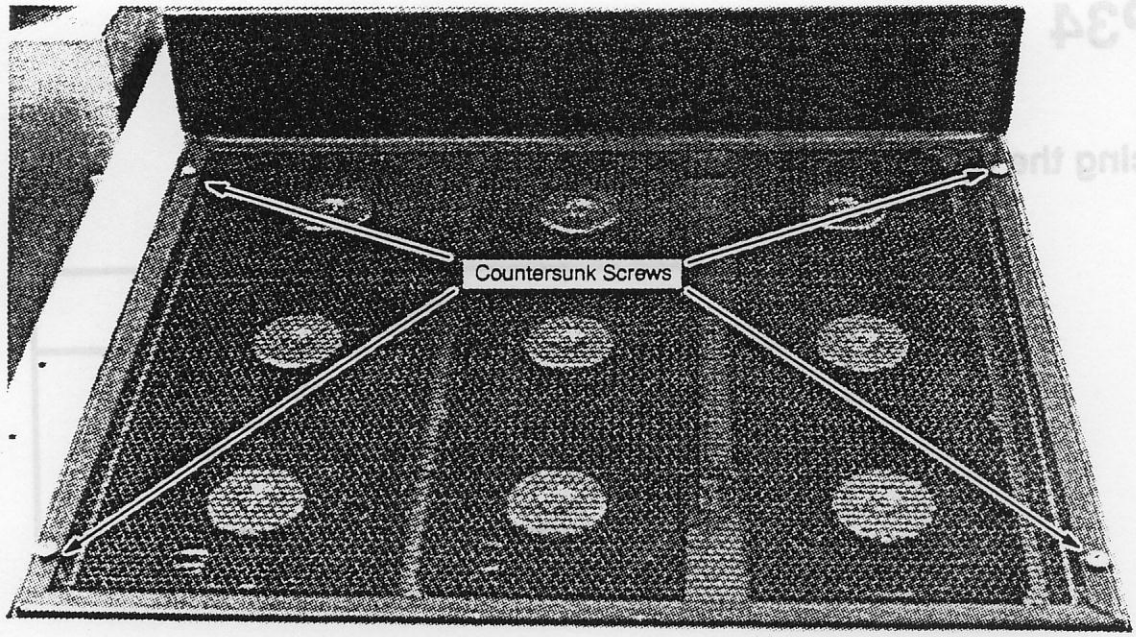


Figure 7-33. Top Fan Tray Perforated Cover

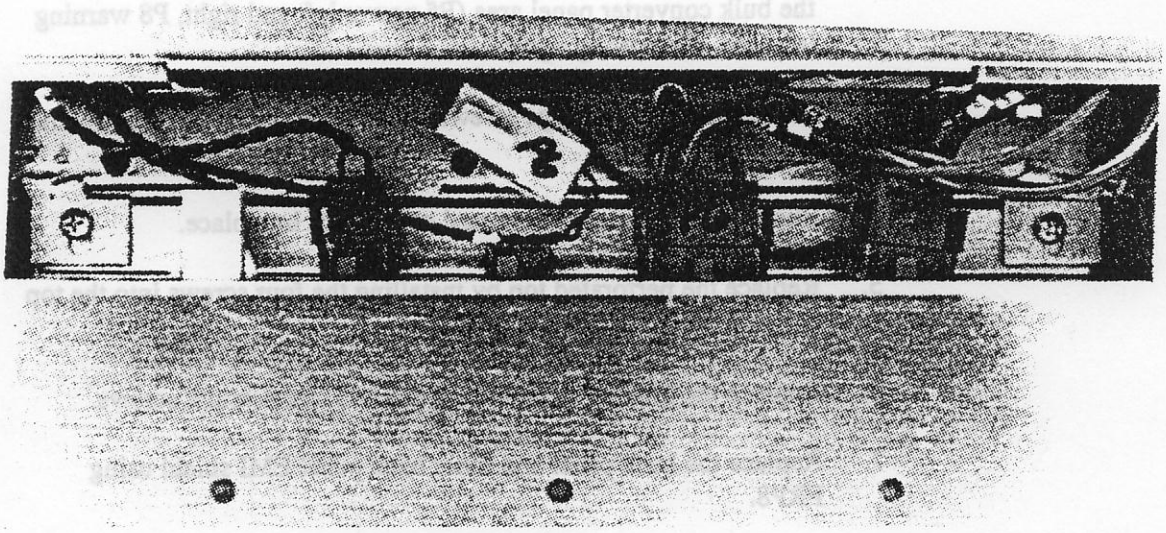


Figure 7-34. Upper Fan Tray Power Plugs

FRP34

Replacing the Upper Fan Tray

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Insert the tray into the chassis.
2. Reconnect the fan power plug and warning signal plug located in the bulk converter panel area (P5 power left and right, P8 warning left, and P7 warning right).
3. Replace the four Phillips screws and four hex stand-off screws into the fan tray.
4. Slide the top fan tray perforated cover back into place.
5. Replace the perforated top by installing the four screws into the top fan tray perforated cover.
6. Replace the grill by reconnecting the two countersunk screws.
7. Replace the back panel and inner back panel EMI shield using FRP8.
8. Power up the system using FRP1.

FRP35

Removing the 8-mm EXABYTE EX-2 Small Computer System Interface (SCSI)

Refer to FRP11 for steps and diagrams if you need information about pulling out the IOS VME card cage.

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2
2. Open the right side panel using FRP5.
3. Remove the IOS tray-retaining screws.
4. Remove all IOS card cage cables that connect to any IOS controllers. The IOS controllers connect to the front of the controller cards. Ensure that all cables are labeled correctly.
5. Ensure that all removed cables are clear, and then pull out the IOS tray to its fully extended and locked position.
6. Remove the SCSI controller cable from the EX-2 drive by using the connector cable ejector tabs. Refer to Figure 7-35.
7. Remove the EX-2 drive power connector shown in Figure 7-36.
8. Remove the four allen screws, two on each side of the drive, and lift out the EX-2 drive.

NOTE: Two of the four screws will be for the retaining screws to the DC inhibit/enable button.

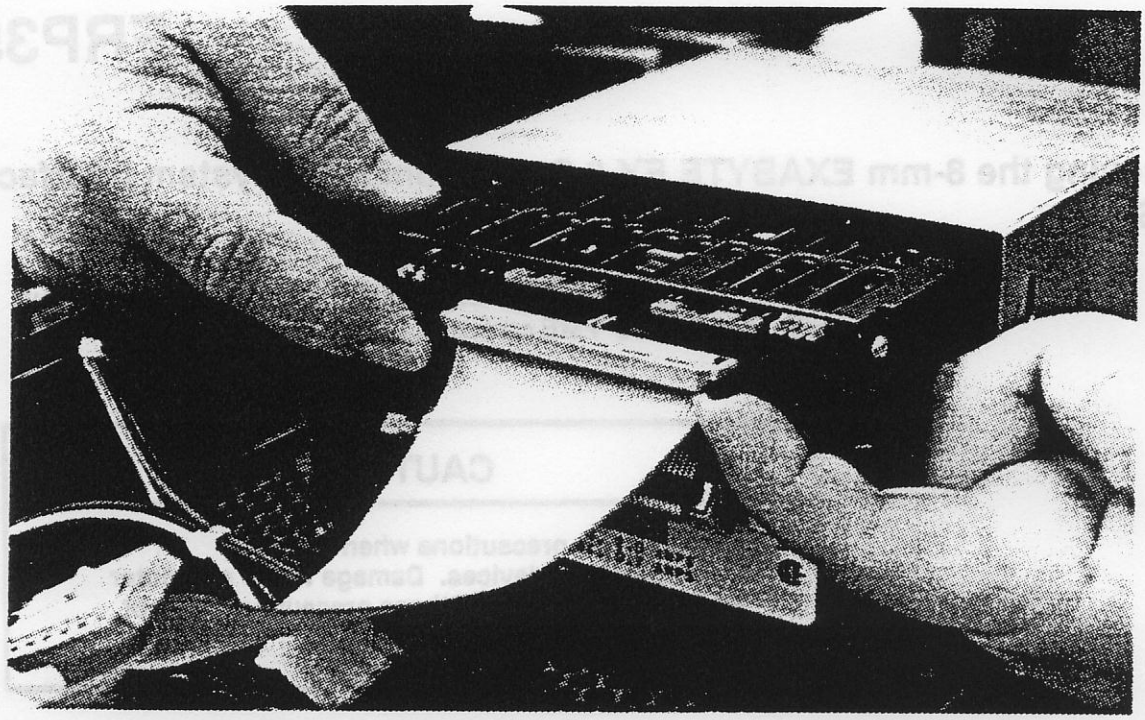


Figure 7-35. EX-2 SCSI Controller Cable

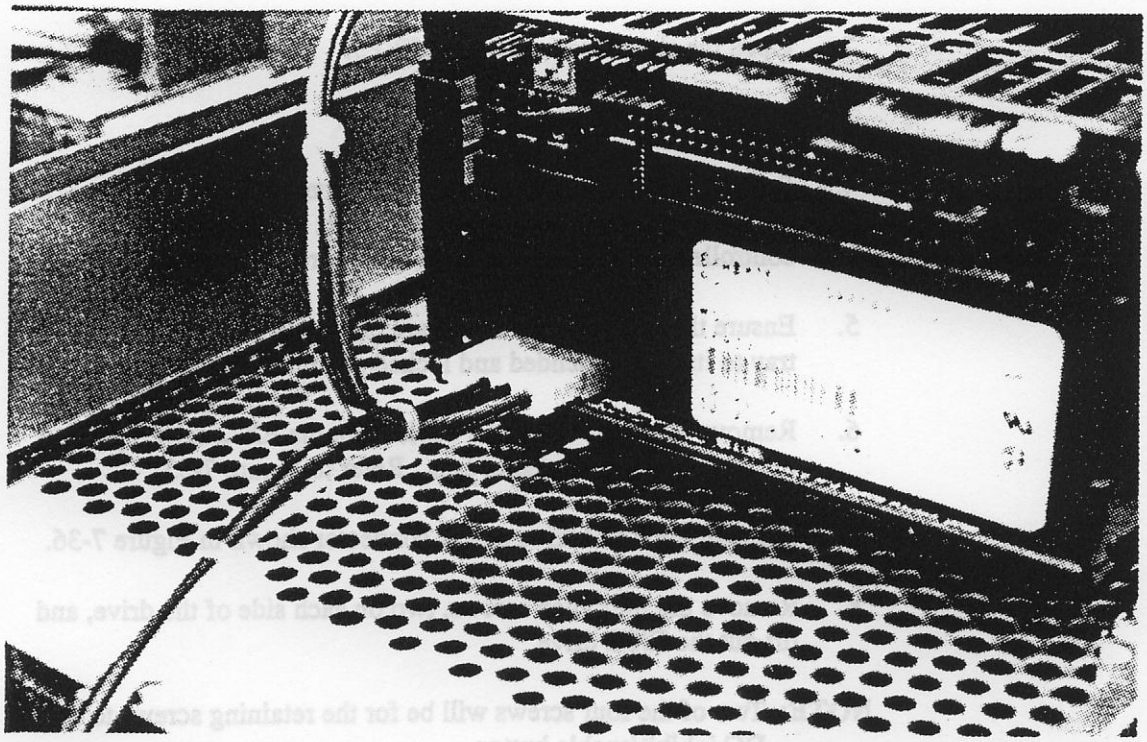


Figure 7-36. EX-2 Drive Power Connector

FRP36

Replacing the 8-mm EXABYTE (EX-2) Small Computer System Interface (SCSI)

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Working at an ESD-safe area, ensure that the replacement drive is configured identically to the drive that you removed.
2. Lift the EX-2 drive and place it in the SCSI.
3. Replace the four allen screws.
4. Replace the SCSI controller cable using the connector cable ejector tabs.
5. Ensure that all cables are clear of any obstruction and then push the IOS tray back into the chassis.
6. Replace all IOS card cage cables, using the labels you made during FRP35.
7. Replace the six IOS card cage retaining screws.
8. Close the right side panel using FRP6.
9. Power up the system using FRP1.

FRP37

Removing the Disk Array Controller (DAC) Board

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Open the side panel using FRP5.
3. Remove the front face panel from the DAC. This is a snap-fit panel. Refer to Figure 7-37.
4. Remove the four screws securing the plastic cover and the DAC tray to the frame and fully extend the DAC. Refer to Figure 7-38 for a diagram of the DAC control panel.
5. Remove the front panel and inner front panel EMI shield using FRP3.
6. Remove the front inner voltage access panel by removing the six screws. Support the weight of the control panel while you lower it to the floor.
7. Ensure that system voltage is at 0 using FRP50.
8. Ensure that all cable locations are labeled on the cable ends, and then disconnect them.
9. Disconnect the power lead and the cable carrier.
10. While supporting the DAC, depress the release tray slider locks. Slide the DAC assembly all the way out of the chassis. Refer to Figure 7-39.

11. Move the DAC boards to the new assembly.

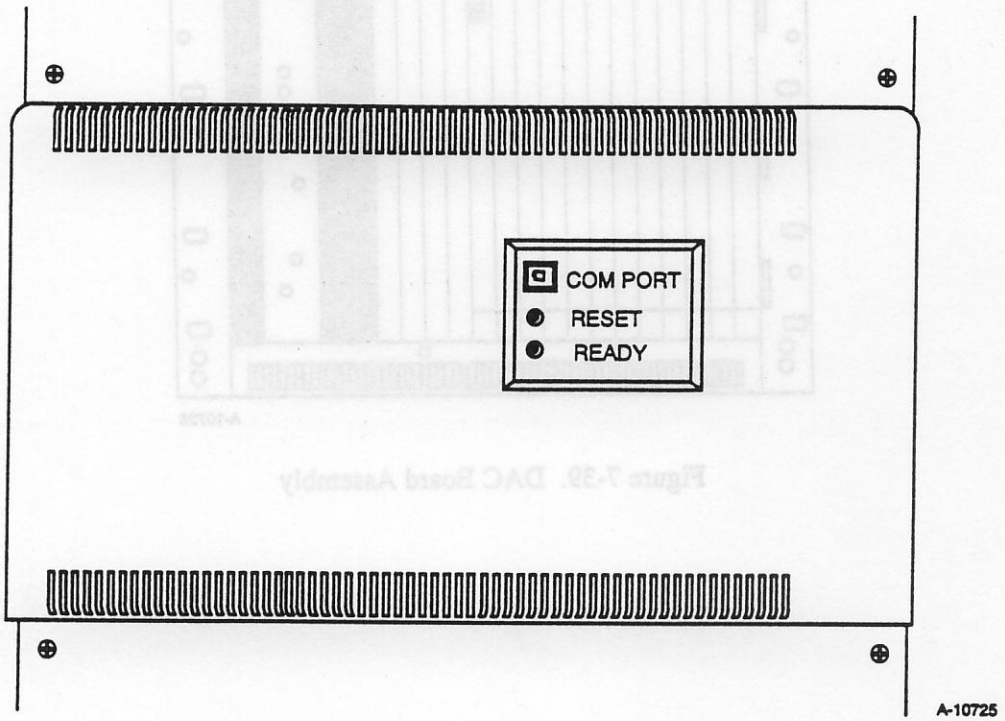


Figure 7-37. DAC Snap-fit Panel

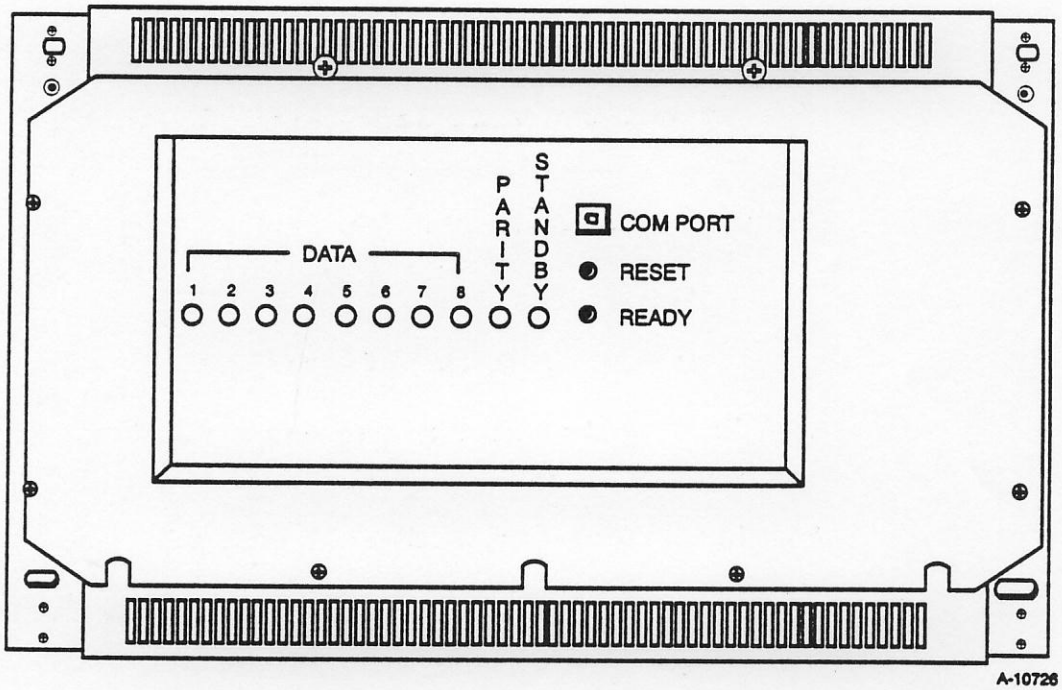


Figure 7-38. DAC Control Panel

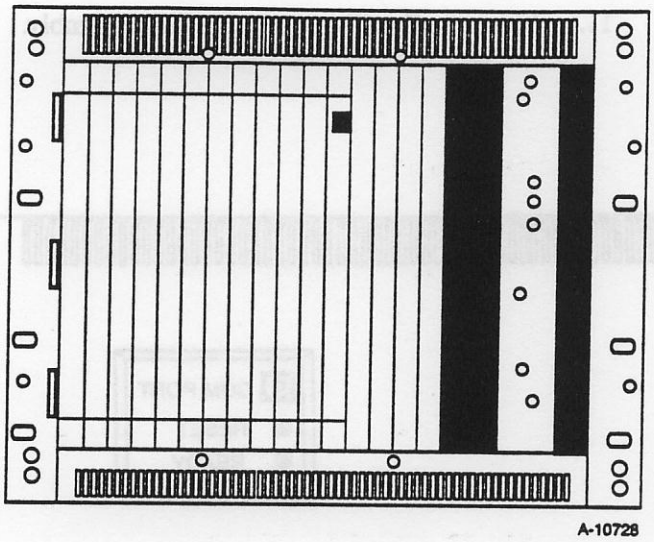


Figure 7-39. DAC Board Assembly

FRP38

Replacing the Disk Array Controller (DAC)

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. While supporting the DAC, push it back into the system.
2. Reconnect the power lead and the cable carrier.
3. Reconnect all cables.
4. Replace the four screws securing the DAC chassis.
5. Replace the snap-fit face panel.
6. Replace the front panel and inner front panel EMI shield using FRP4.
7. Replace the side panel using FRP6.
8. Power up the system using FRP1.

FRP39

Removing the Peripheral Equipment Drawer 3 Tray Power Supply

This power supply is shared by all drives in the peripheral equipment drawer 3 (PE-3) drawer. This power supply is probably faulty when all of the drives in the drawer do not work.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

1. Power down the system using FRP2.
2. Open the side panel using FRP5.
3. Attach the ESD wrist strap to earth ground point.
4. Remove the four tray-retaining screws. Refer to Figure 7-40.
5. Remove the four power-supply retaining screws. Refer to Figure 7-41.
6. Extend the disk tray carefully, using the slide handles.

7. Remove the two retaining screws from the disk tray top cover. (Refer to Figure 7-41.) Remove the cover by lifting the front up and out to disengage the rear location tabs.

8. Remove the two front plugs and one rear plug from the power-supply assembly. Refer to Figure 7-42.

9. Pull the assembly out from the front of the tray.

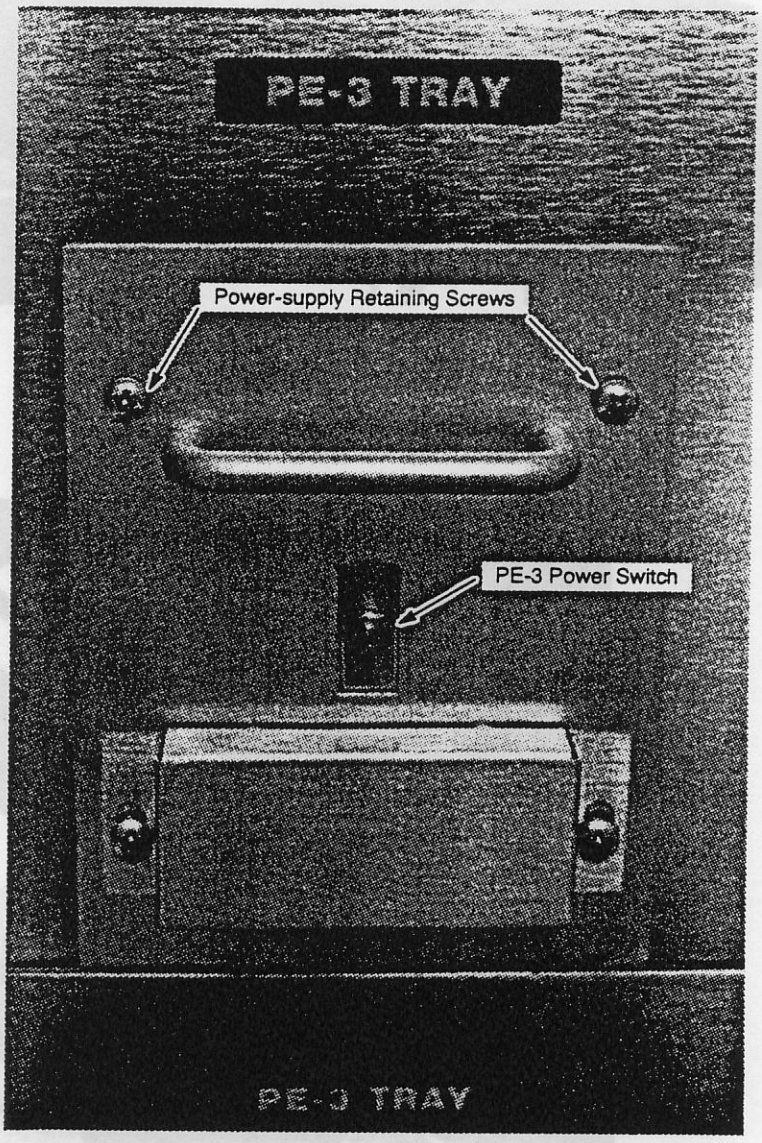


Figure 7-40. PE-3 Drawer

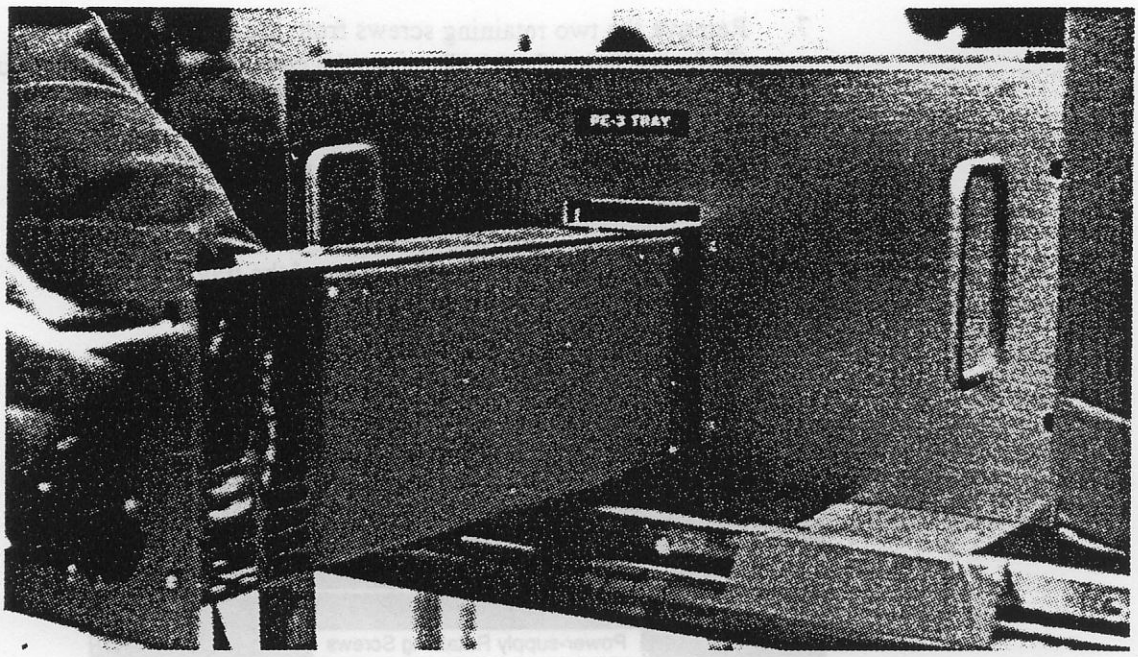


Figure 7-41. PE-3 Power Supply

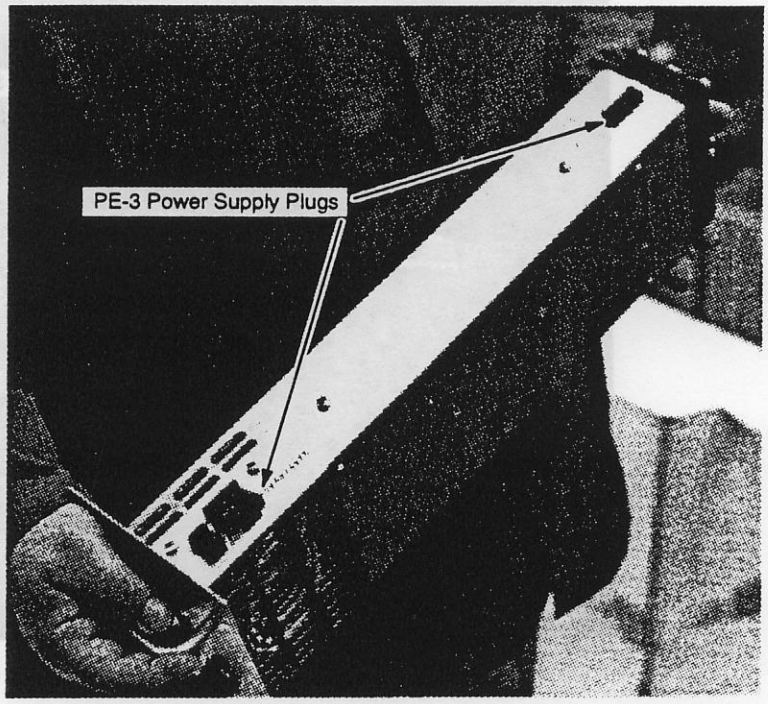


Figure 7-42. PE-3 Power Supply Plugs

FRP40

Replacing the Peripheral Equipment Drawer 3 Tray Power Supply

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Insert the replacement disk tray power-supply assembly.
2. Reinstall the two front plugs and one rear plug in the power-supply assembly.
3. Replace the top cover by engaging the location tabs in the rear cutouts. Lower the front and secure it with the two screws removed in Step 7 of FRP39.
4. Slide in the tray after replacing the two slider latches.
5. Secure the power supply using the four screws removed in Step 5 of FRP39.
6. Secure the tray using the four screws removed in Step 4 of FRP39.
7. Replace the side panel using FRP6.
8. Power up the system using FRP1.

FRP41

Removing the Enhanced Small Disk Interface (ESDI)

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the PE-3 drawer by placing the 0/1 button to a 0 to turn off its power supply.
2. Open the side panel using FRP5.
3. Connect your ESD wrist strap to the nearest earth ground point.
4. Remove the four tray-retaining screws from the IOS VME.
5. Extend the tray fully by carefully pulling on the two tray handles.
6. Remove the two retaining-tray screws, one on each side. Refer to Figure 7-43.
7. Remove all of the cables from the drive to be replaced and push them to the side to allow drive removal. You may have to remove one or more power plugs from other drives in order to have sufficient space to clear the drive. Refer to Figure 7-44.
8. Using the drive handle, pull the drive up and out of the tray. Refer to Figure 7-45. Avoid carrying the drive by the handle, as it may fall. Support the drive with two hands when possible.
9. Transfer the drive-mounting hardware and handle to the replacement drive. Work in an ESD-safe work area.

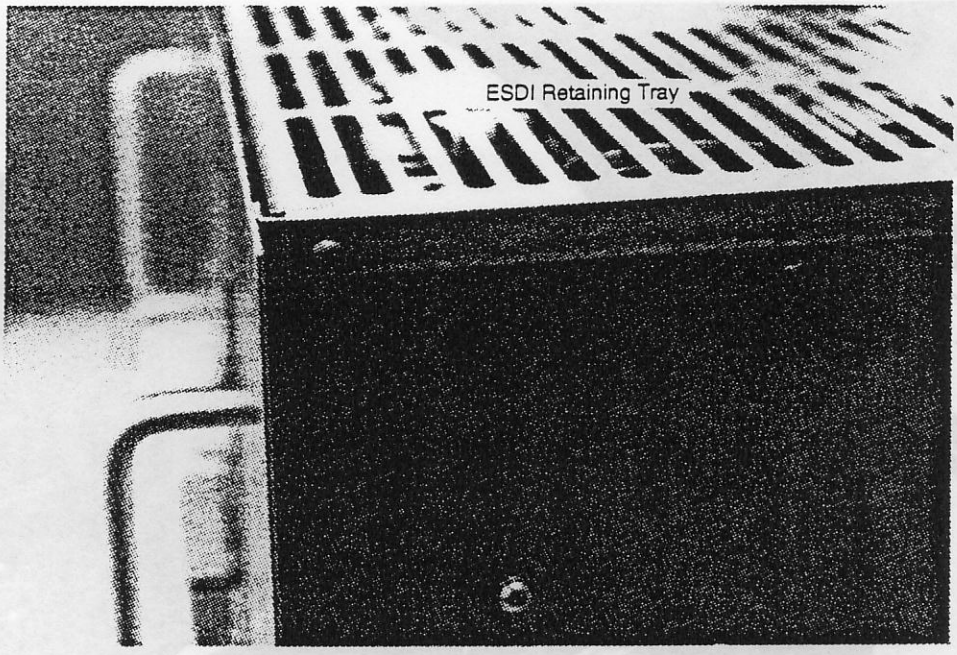


Figure 7-43. ESDI Retaining Tray

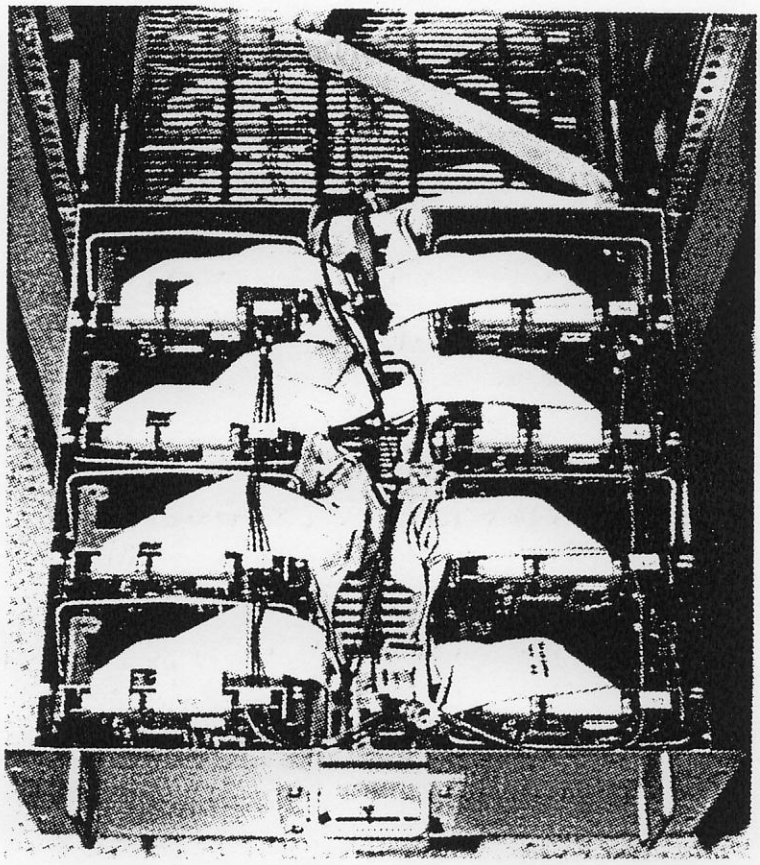


Figure 7-44. ESDI Cables

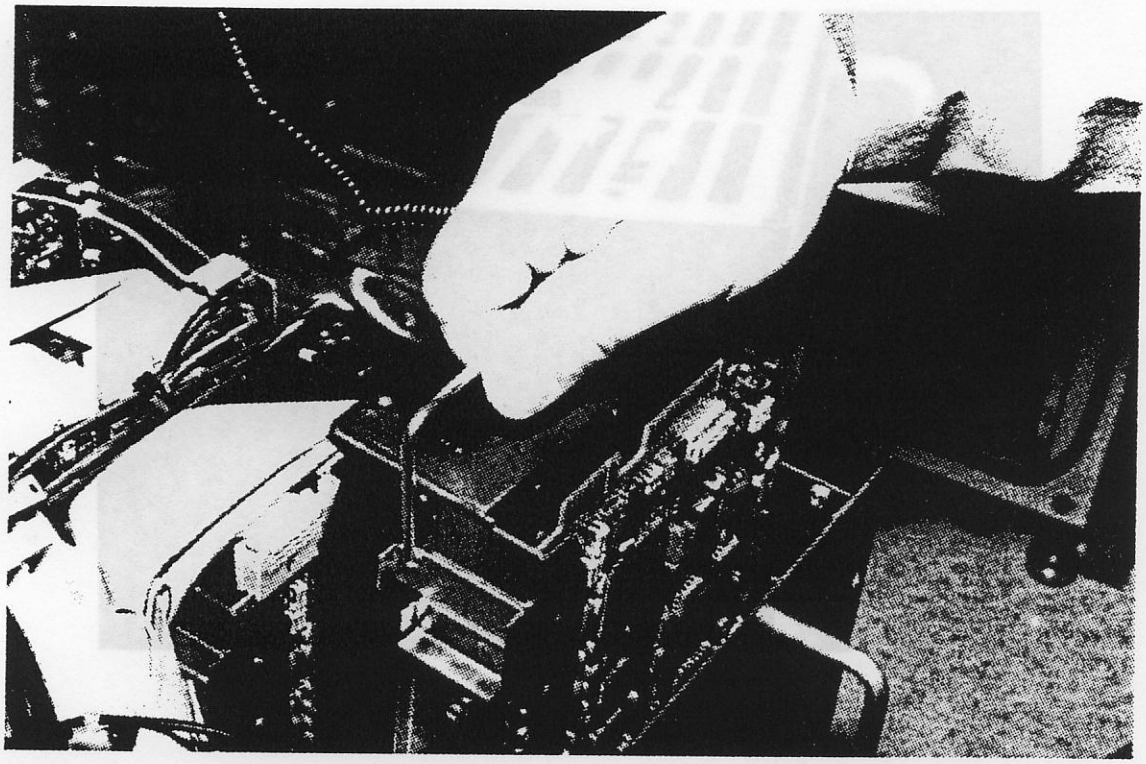


Figure 7-45. ESDI Drive Handle

FRP42

Replacing the ESDI

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Avoid carrying the drive by the handle alone; slide the replacement drive into the mounting blocks in the tray.
2. Reconnect all cables. Ensure that the routing is correct and orderly.
3. Place the tray-cover locating tabs into the cutouts in the back of the tray. Lower the front of the tray cover and secure it with the two screws removed in Step 6 of FRP41. Ensure that no cables are trapped.
4. Slide the tray back into the chassis. Depress the slider locking latches on either side of the tray.
5. Secure the tray to the chassis with the four screws removed in Step 4 of FRP41.
6. Replace the side panel using FRP6.
7. Power up the PE-3 drawer by placing the power supply switch to a 1.

FRP43

DR-1 Keying

The removable drive (DR-1) for the system will be keyed when the system is initially shipped but will not be keyed when a replacement is shipped from Logistics. The system will ship with a keying kit. The keying scheme will be recorded on the front of the data shuttle and the DR-1. Write on the tray the keying position assigned to that drive. This procedure includes the DR-1 top panel removal and replacement.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.

NOTE: The following step requires two people.

2. Remove the data shuttle cover by removing the top three screws on the rail and loosening the bottom three. A second person should support the drive while the first person loosens the bottom three screws. Refer to Figure 7-46.

3. Remove the top cover to gain access to the hex sleeve.

4. Remove the "C" ring from the hex sleeve assembly.

5. Remove the hex sleeve from the panel assembly.

6. Position the hex sleeve (Figure 7-47) according to the combination assigned to that drive. An example of keying is shown in Figure 7-48. The combination in the example is 1/1 (left set of keys) and 5/3 (right set of keys).

7. Insert the hex sleeve back into the panel assembly.

8. Snap the "C" ring over the hex sleeve assembly.

NOTE: The following step requires two people.

9. Replace the top cover.

   a. Insert the panel cover over the assembly.

   b. Replace the three screws on the rail.

   c. Tighten the bottom three screws.

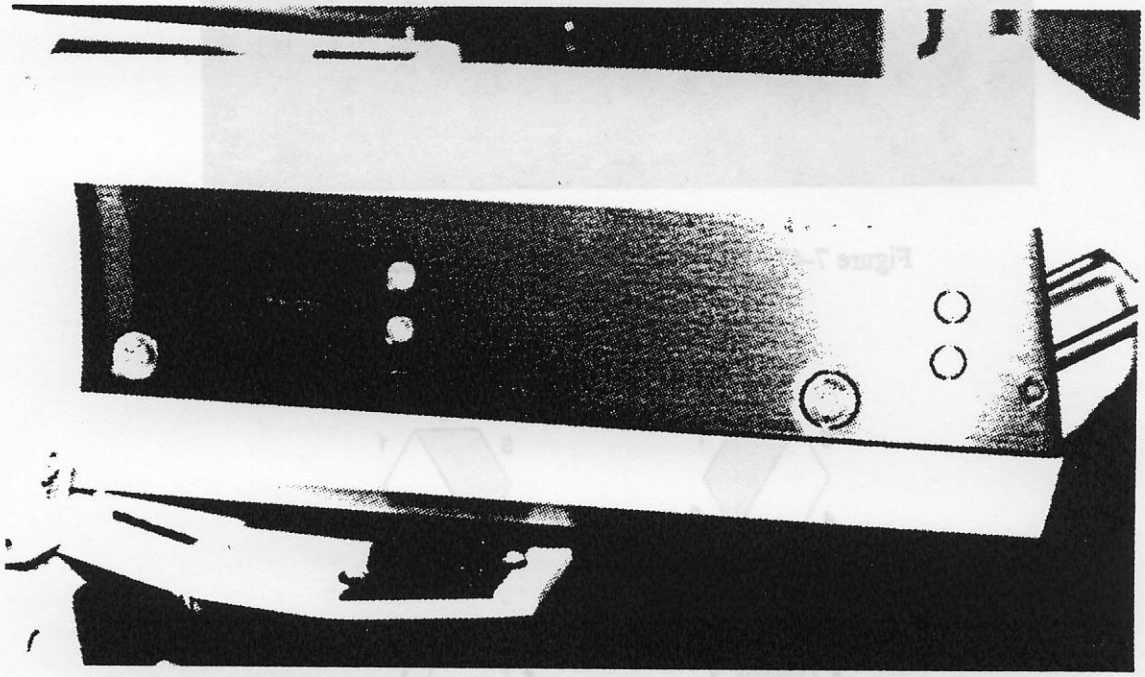


Figure 7-46. Removing DR-1

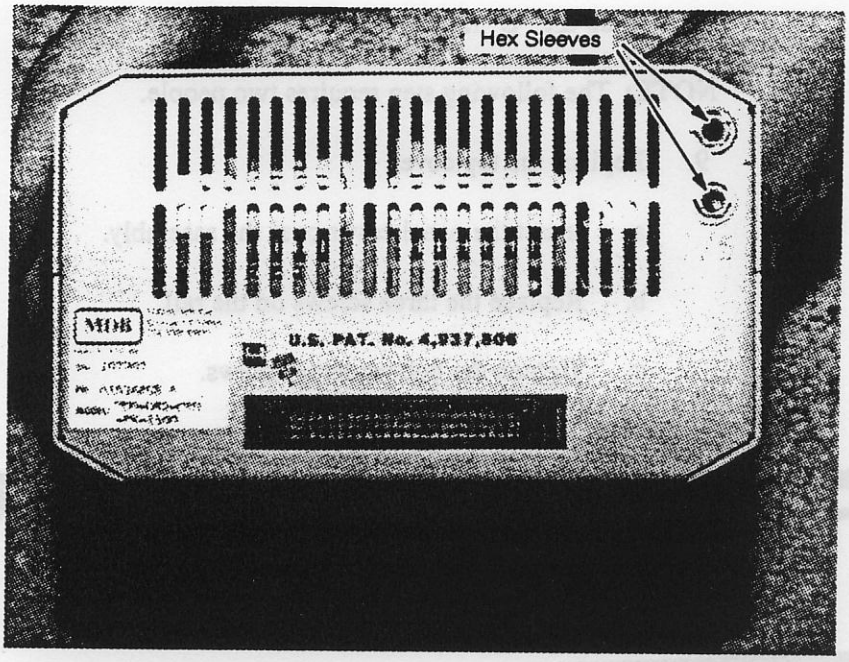


Figure 7-47. DR-1 Data Shuttle (Inside Back View)

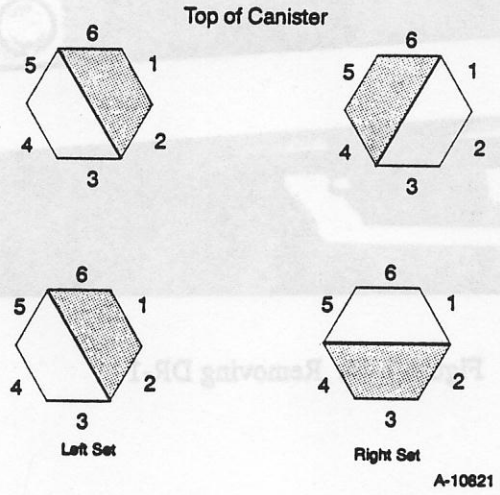


Figure 7-48. DR-1 Keying Example

FRP44

Removing the Intelligent Peripheral Interface Disk Drive

The individual intelligent peripheral interfaces (IPIs) are the disk drives used in the disk drive-4 (DD-4) subsystem in the peripheral equipment-4 (PE-4) drawer. Use error logs and run the IPItest to determine whether the IPI drive is defective.

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Shut off the power to the PE-4 drawer by moving the 0/1 button to the 0 position. Refer to Figure 7-49.
2. Remove the four PE-4 drawer retaining screws that are shown in Figure 7-50 to remove the top trim.
3. Extend the drawer.
4. Remove the five screws along each edge of the top cover.
5. Remove the two screws attached to each individual drive. Refer to Figure 7-51.
6. Lift off the tray.
7. Disconnect the three ribbon cables from the front of the drive being replaced. Refer to Figure 7-51.
8. Remove the two screws on the bottom of the drive to be replaced.
9. Lift the drive partially out of the drawer. It may be necessary to disconnect the power cables from the power supplies and move them out of the way first.

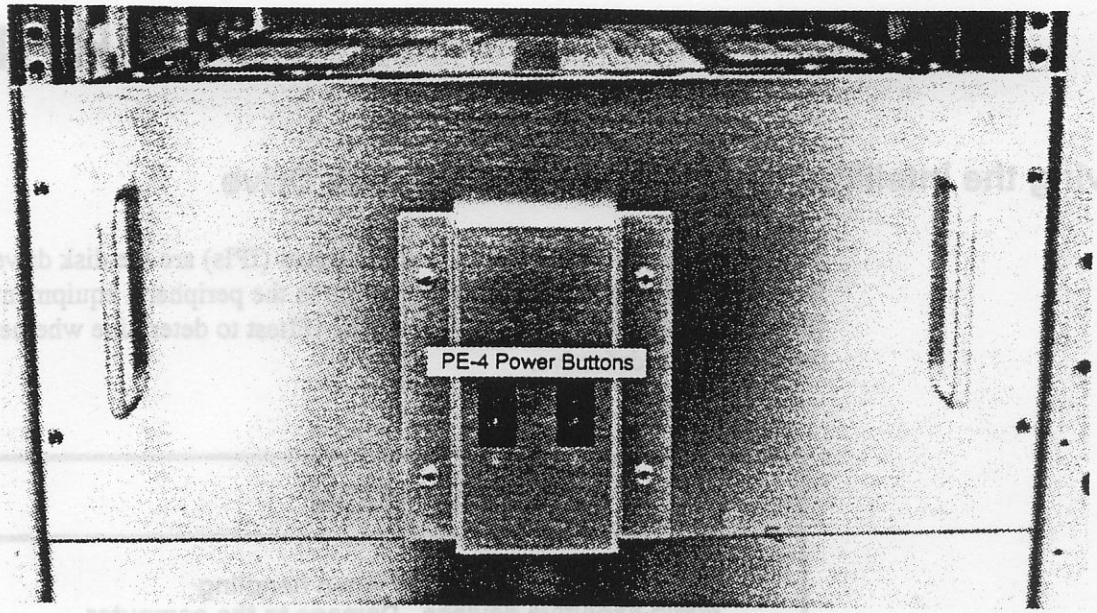


Figure 7-49. PE-4 Drawer

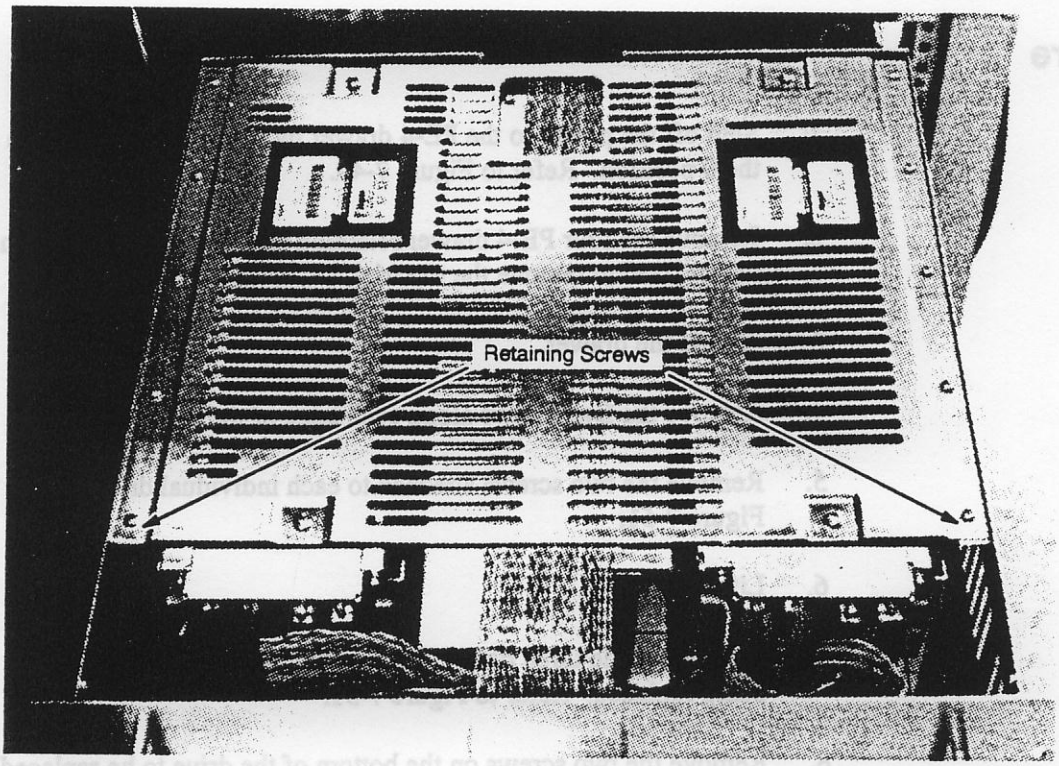


Figure 7-50. PE-4 Drawer Trim

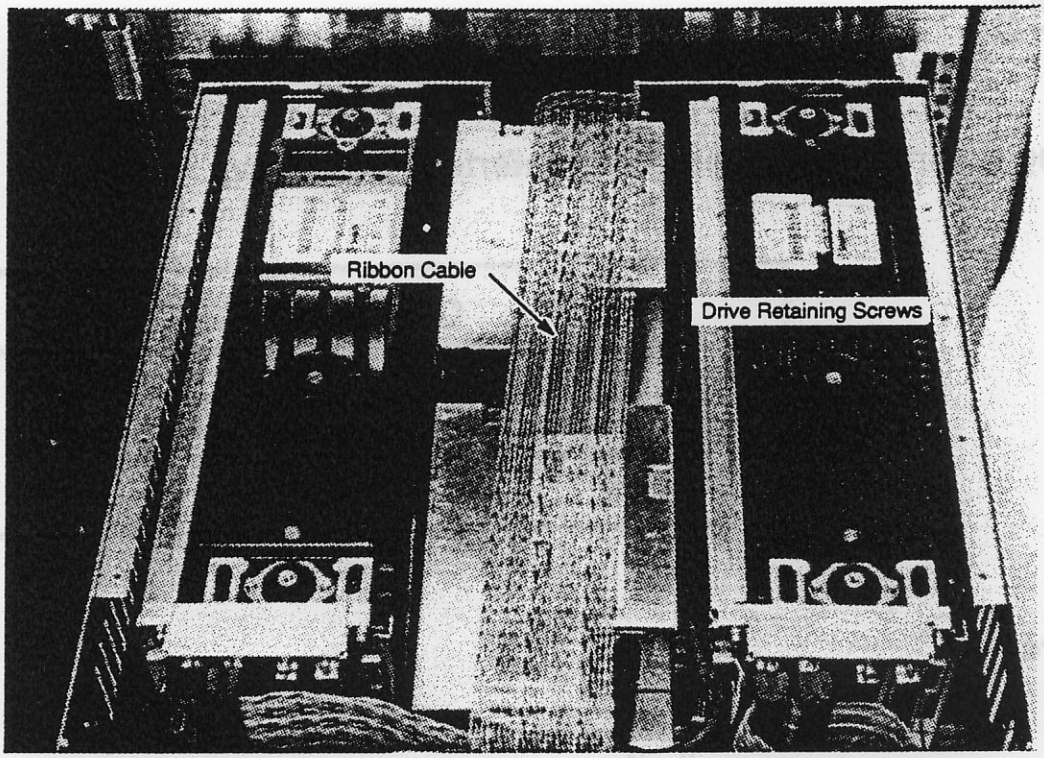


Figure 7-51. IPI Drives and Ribbon Cables

FRP45

Replacing the Intelligent Peripheral Interface Disk Drive

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Insert the new drive and replace the power cables and power supplies if necessary.
2. Replace the two screws on the bottom of the new drive.
3. Reconnect the three ribbon cables to the new drive.
4. Replace the tray.
5. Replace the two screws attached to each drive.
6. Replace the IPI top cover by replacing ten screws.
7. Replace the four PE-4 drawer screws.
8. Push the drawer back into the chassis.
9. Turn on the power to the PE-4 drawer by placing the power supply button to a 1.

FRP46

Removing the Intelligent Peripheral Interface Power Supply

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Remove the hex screw securing the ground wire to the front of the drive.
3. Lift the IPI power supply completely out of the drawer.

FRP47

Replacing the Intelligent Peripheral Interface Power Supply

CAUTION
Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Place the new power supply in the drawer.
2. Attach the power-supply ground wire by securing the hex screw.
3. Power up the system using FRP1.

FRP48

Splitting a Multicabinet System

The following procedure lists the steps required to separate a cabinet from the mainframe cabinet.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Power down the system using FRP2.
2. Lift off and remove all trim.
3. Remove the bolts that connect the cabinets together at the top of the system.
4. Remove the bolts (hose clamps) that connect the cabinets together at the bottom of the system.
5. Raise the leveling pads on cabinets 2, 3, or 4.
6. Push the expansion cabinet(s) away from the mainframe cabinet.

FRP49

Reconnecting a Multicabinet System

Procedure

1. Push the expansion cabinet towards the mainframe.
2. Lower the leveling pads on the expansion cabinets.
3. Reconnect the hose clamps that connect the cabinets together at the bottom of the system.
4. Reconnect the bolts that connect the cabinets together at the top of the system.
5. Replace all trim.
6. Power up the system using FRP1.

FRP50

Performing a Voltage Check

It is necessary when working with any component associated with the high-voltage circuits to perform a voltage check after you have powered down the system to ensure that there is no current in the system. You will need a digital voltmeter (DVM) to take this measurement.

CAUTION

Observe ESD precautions when handling static-sensitive devices. Damage to the computer equipment will result if these precautions are not followed.

Procedure

1. Remove the back panel assembly using FRP7.

DANGER

Wait for the system to completely power down before you touch any components associated with the high-voltage circuits. Verify power loss by performing a voltage check; failure to do so will result in death or serious injury.

2. Remove the vertical wireway cover by removing its retaining screws.
3. Attach a DVM to an unused or disconnected bus. There are exposed buses located inside the vertical wireway.
4. Ensure that the reading on the DVM equals 0 volts. If it does not, wait one minute and take another reading.
5. When the DVM reading equals 0 V, proceed with the recommended maintenance procedure.

8 REMOTE SUPPORT

This section documents the Remote Support capabilities for the CRAY Y-MP EL computer system. The Remote Support 3.0 release, in conjunction with the SMARTE 2.0 release, provide remote access and testing capabilities. Refer to the *System Maintenance and Remote Testing Environment (SMARTE) User's Guide*, publication number SPM-1017 2.0 for complete information about the SMARTE system and running SMARTE remotely.

NOTE: Text and messages displayed on a screen appear in `courier` font. Commands and options that the user should enter appear in **`courier bold`** type font. Courier *`italic`* indicates a variable or user-supplied command or option.

The Remote Support System

Remote Support 3.0 is a hardware platform and software package that enables you to troubleshoot, support, monitor, and maintain the CRAY Y-MP EL computer system from a remote location. The Remote Support system connects the MWS-EL at the site to a Service Center workstation (through a Communication Hub) using the Telebit NetBlazer IP router and Microcom modem. The term *Service Center* is used to describe a location from which remote service is provided to sites. The term *Communication Hub* is used to describe a location that provides a communication link between sites and Service Centers.

Because you can log on to the maintenance workstation of the site, you can perform any of the following Remote Support maintenance functions from a Service Center workstation.

- Diagnose system failures
- Perform hardware maintenance concurrent with customer operations
- Degrade system components
- Transfer files
- Install software modifications

- Participate in training and lab exercises from an education center
- Monitor hardware performance

The Remote Support package enables support personnel to dial into the site (by first dialing into a Communication Hub gateway), log on to the MWS-EL, and run maintenance tools. The tools run on the MWS-EL and are displayed on a Service Center display screen as they would be on-site. The term *Communication Hub gateway* is used to describe the workstation of a Communication Hub used to gain access to the sites from Service Centers.

The Remote Service Environment

This subsection briefly describes the remote service environment. This environment is aimed at providing efficient and secure remote support. This environment also facilitates the use of Remote Support hardware and software tools and other tools, such as the SMARTE online maintenance system. Please note that this environment will continue to evolve. The following information provides information about the current remote service environment.

Figure 8-1 is an example of a CRAY Y-MP EL remote support site.

Telebit NetBlazer

The Telebit NetBlazer (Figure 8-2) is a multipurpose Transmission Control Protocol/Internet Protocol (TCP/IP) device used as a dial-up router for transferring IP datagrams over a public telephone or X.25 network. The primary function of the NetBlazer is to route IP datagrams to a host on a network connected directly to the NetBlazer or through the public-switched telephone network to a host connected to another NetBlazer.

Network users are unaware of most NetBlazer operations. The NetBlazer performs all tasks needed to establish a remote connection without requiring user interaction. For example, when a user starts a telnet session to a remote location, the NetBlazer automatically establishes a connection to the location.

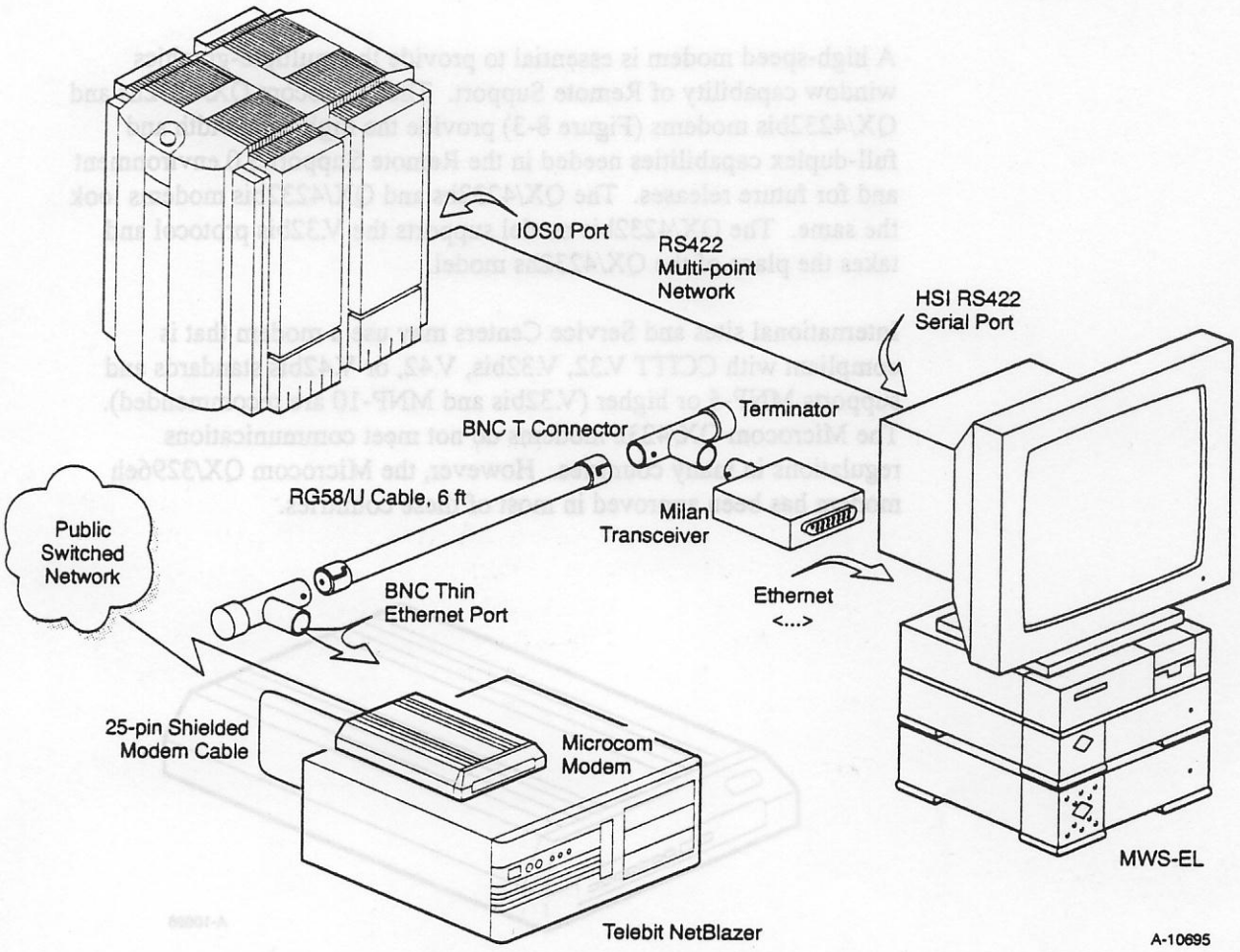


Figure 8-1. CRAY Y-MP EL Remote Support Environment

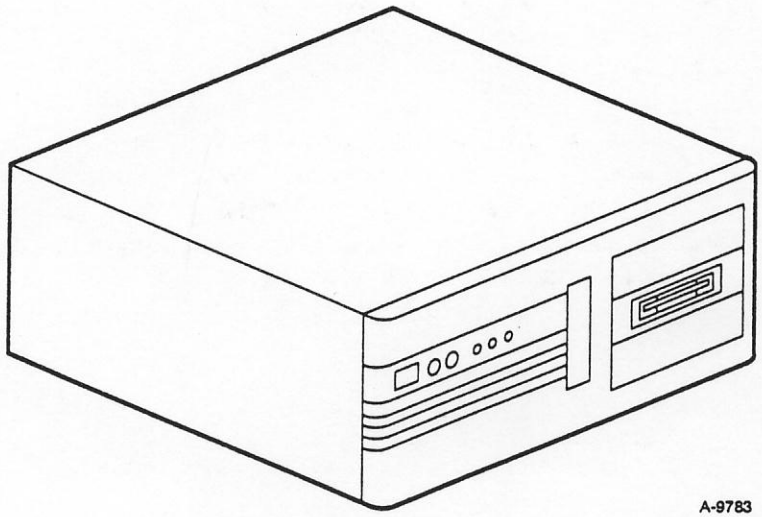


Figure 8-2. Telebit NetBlazer

Microcom Modem

A high-speed modem is essential to provide the multiple-graphics window capability of Remote Support. The Microcom QX/4232hs and QX/4232bis modems (Figure 8-3) provide the high bandwidth and full-duplex capabilities needed in the Remote Support 3.0 environment and for future releases. The QX/4232hs and QX/4232bis modems look the same. The QX/4232bis model supports the V.32bis protocol and takes the place of the QX/4232hs model.

International sites and Service Centers may use a modem that is compliant with CCITT V.32, V.32bis, V.42, or V.42bis standards and supports MNP-5 or higher (V.32bis and MNP-10 are recommended). The Microcom QX/4232 modems do not meet communications regulations in many countries. However, the Microcom QX/3296eh modem has been approved in most of these countries.

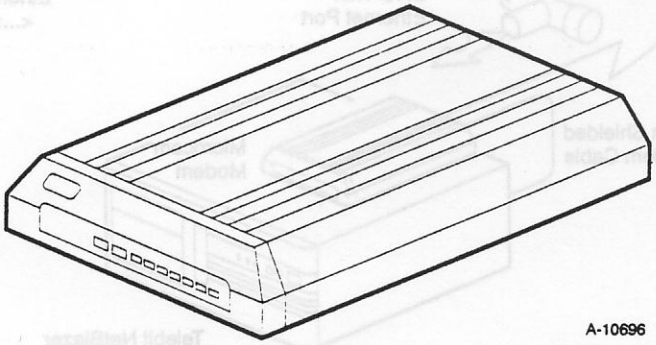
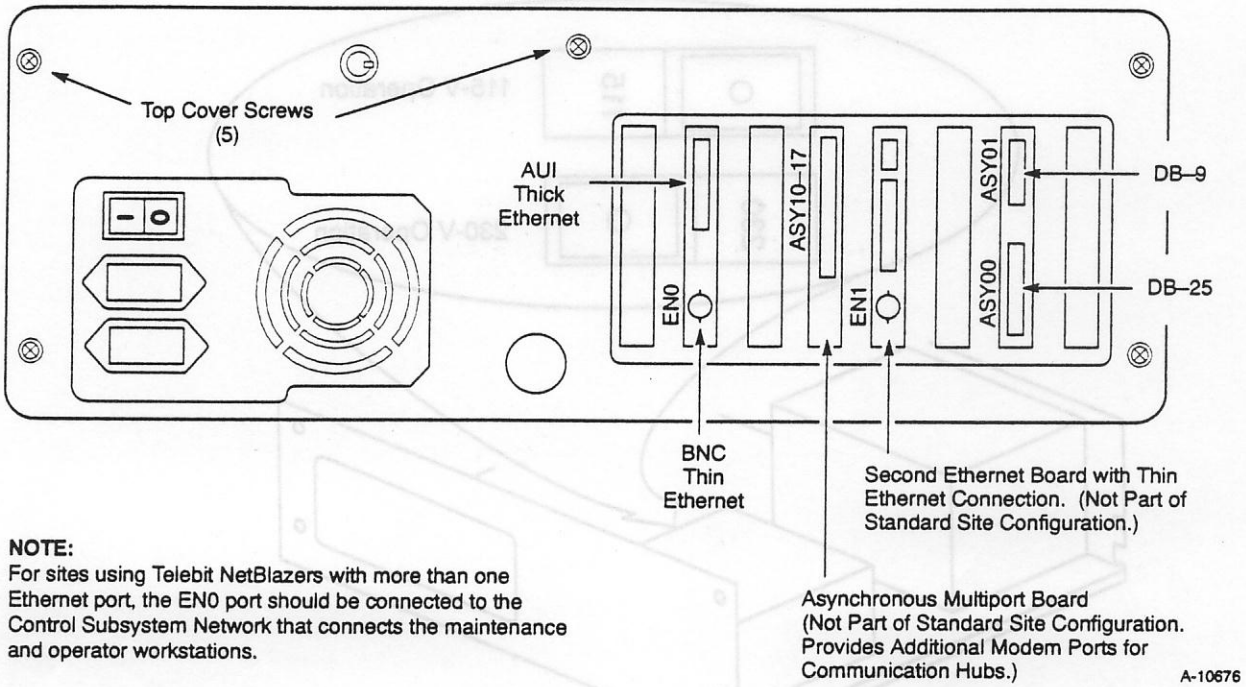


Figure 8-3. Microcom QX/4232 Modem

Cable Connections

Figure 8-4 illustrates cable connections for the Telebit NetBlazer. Figure 8-5 illustrates how to connect the Ethernet dual-port transceiver. Refer to Figure 8-11 for an illustration of the Microcom Modem.



NOTE:
For sites using Telebit NetBlazers with more than one Ethernet port, the EN0 port should be connected to the Control Subsystem Network that connects the maintenance and operator workstations.

Figure 8-4. Telebit NetBlazer Board Placement and Cable Connections

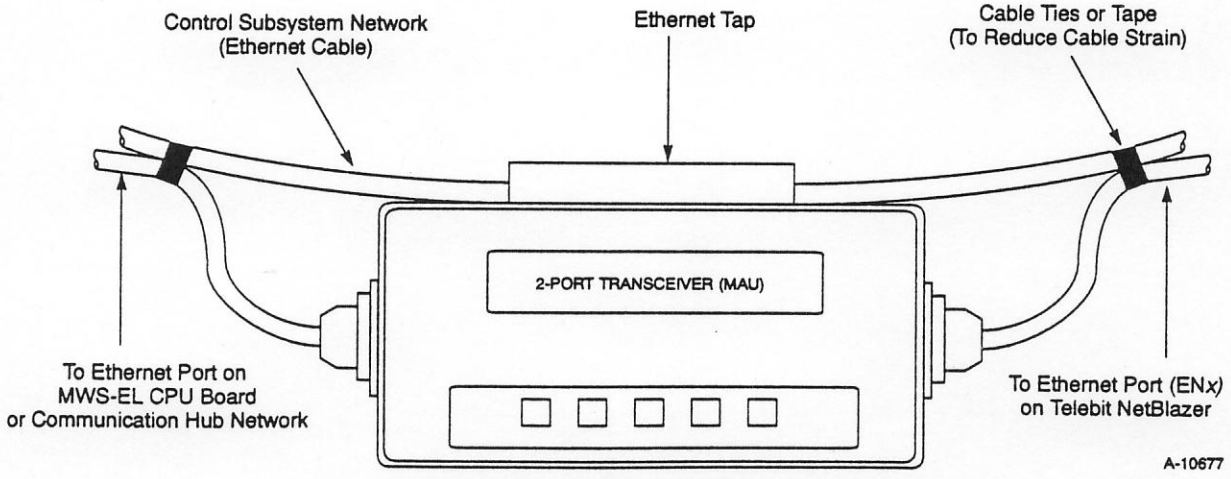


Figure 8-5. Ethernet Dual Port Transceiver

Telebit NetBlazer Power-supply Voltage Switch

The voltage switch on the Telebit NetBlazer power supply must be set to the AC voltage at your location. Refer to Figure 8-6. Remove the five cover screws to access the voltage switch.

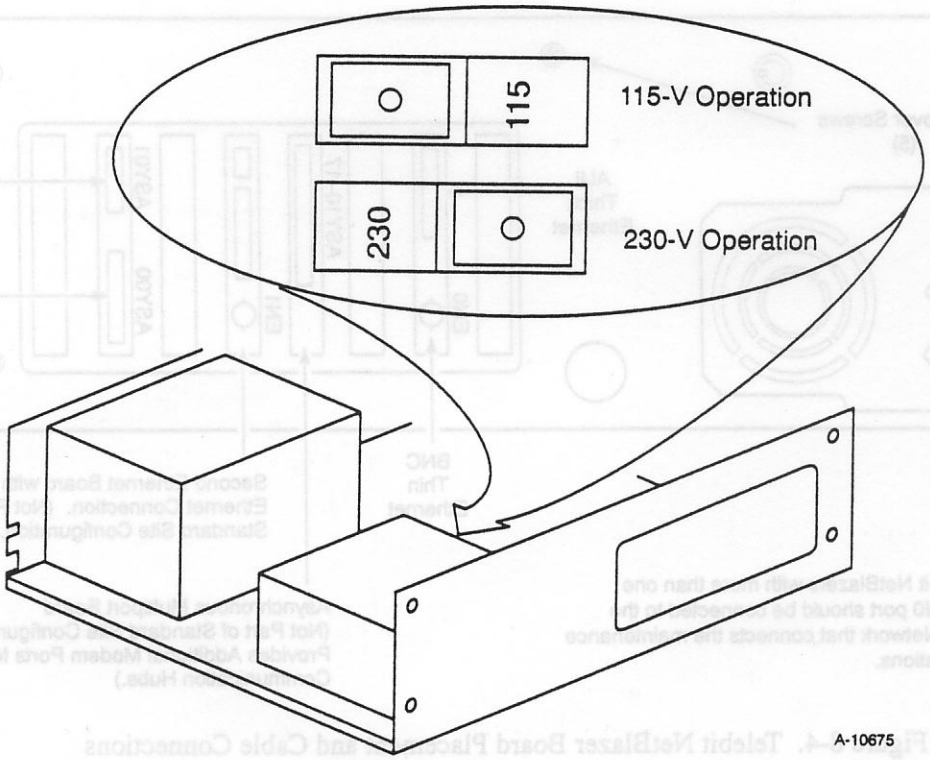


Figure 8-6. Telebit NetBlazer Power-supply Voltage Switch

Telebit NetBlazer Board Configuration

Figure 8-7 and Figure 8-8 illustrate jumper pin connections and switch settings as they appear on configured boards of the Telebit NetBlazer.

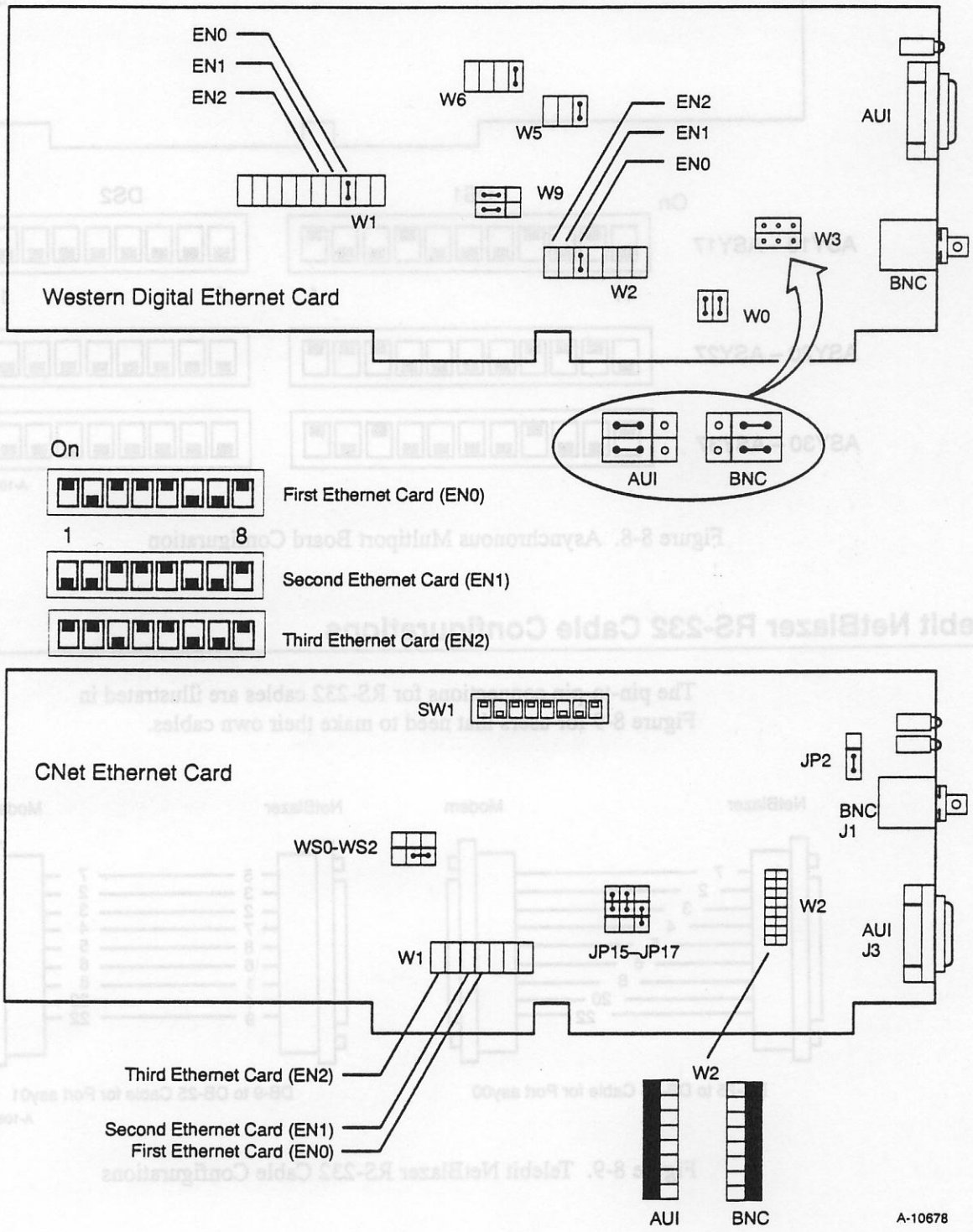


Figure 8-7. Telebit NetBlazer Ethernet Board Configurations

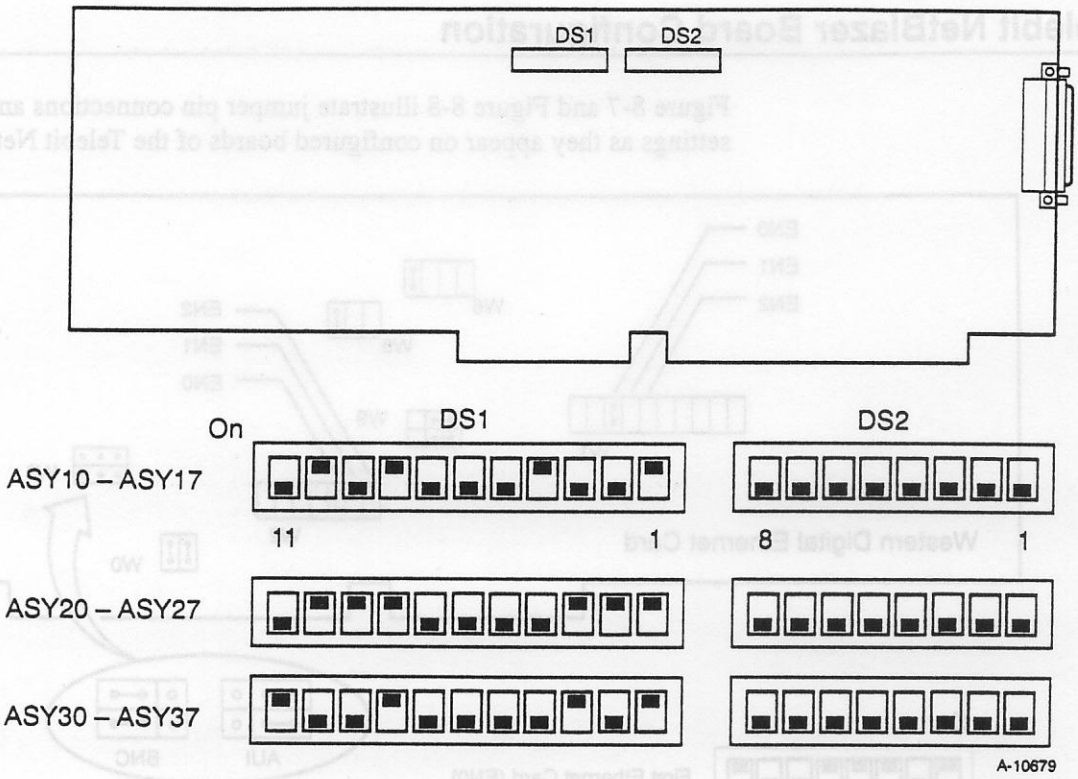


Figure 8-8. Asynchronous Multiport Board Configuration

Telebit NetBlazer RS-232 Cable Configurations

The pin-to-pin connections for RS-232 cables are illustrated in Figure 8-9 for users that need to make their own cables.

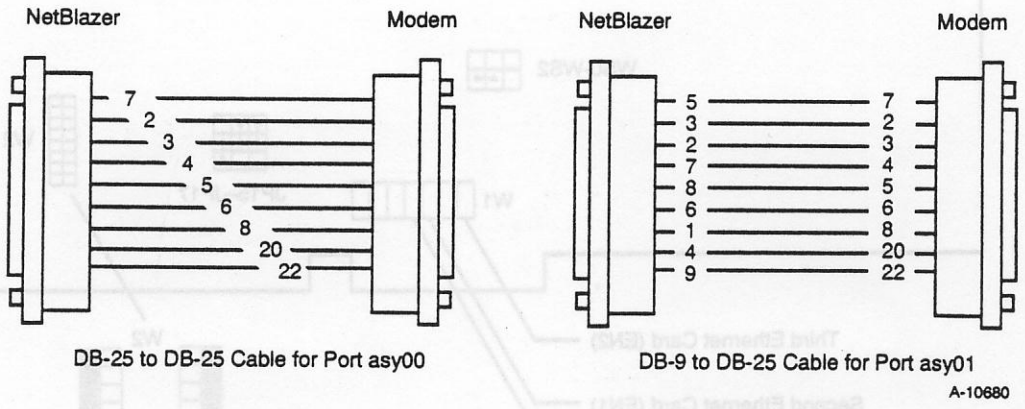


Figure 8-9. Telebit NetBlazer RS-232 Cable Configurations

Configuring the Microcom QX/4232hs Modem

Use the following procedure to configure the Microcom QX/4232hs modem. If you don't have a female DB-25 to male DB-25 modem cable, you can make your own by wiring together the pins shown in Figure 8-10; each wire is a straight pin-to-pin connection.

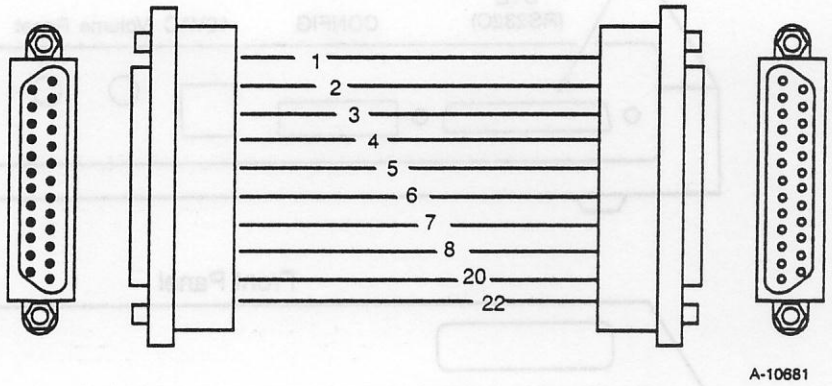


Figure 8-10. Microcom DB-25 Male-to-Female Cable Pin Connections

Refer to Figure 8-4 and Figure 8-11 for diagrams that show Telebit NetBlazer and Microcom modem connectors.

1. Position the T/D and O/A buttons in the Out (on) position.
2. Remove the plastic front panel cover on the front of the modem to access the front configuration switch.
3. Connect the power pack cord to the modem and plug the 19-Vac power pack into an AC outlet.
4. Connect a telephone cable between the To Jack connector on the back of the modem and a data telephone line jack.
5. Connect a shielded RS-232 cable from the DTE connector on the back of the modem to the ASY00 or ASY01 connector on the back of the Telebit NetBlazer.
6. Verify that the power lamp (PWR) on the front of the modem is illuminated.
7. Set the front and back configuration switches as shown in Figure 8-12.

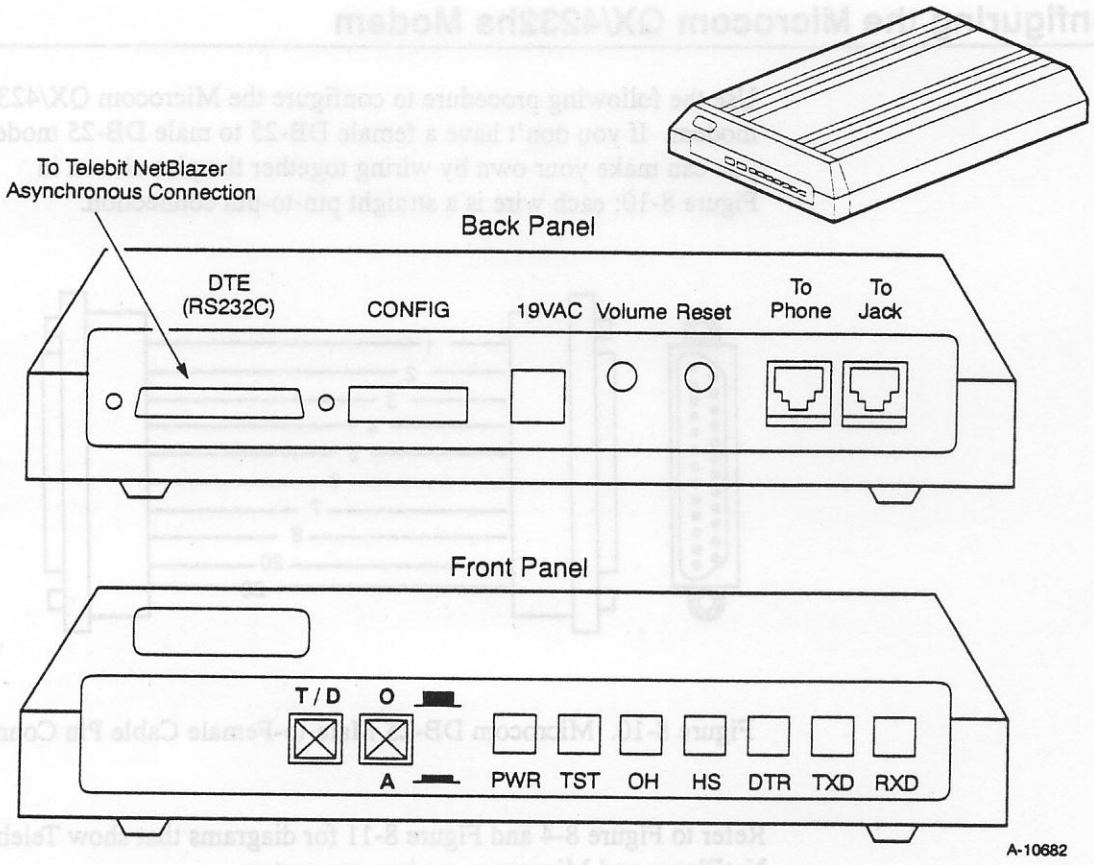


Figure 8-11. Microcom QX/4232 Modem Front and Back Panels

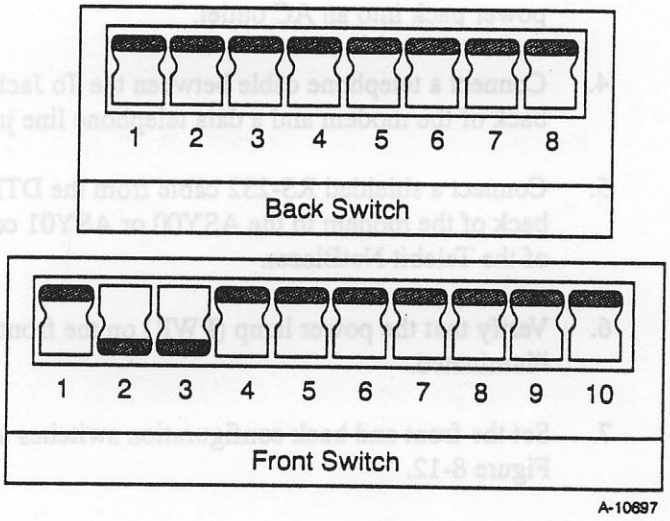


Figure 8-12. Switch Settings, Step 7

8. Press the Reset button on the back of the modem and wait for the TST lamp on the front of the modem to go out. This sets the AT mode extended switches in the Microcom modem.

9. After resetting the modem, reset the configuration switches as shown in Figure 8-13.

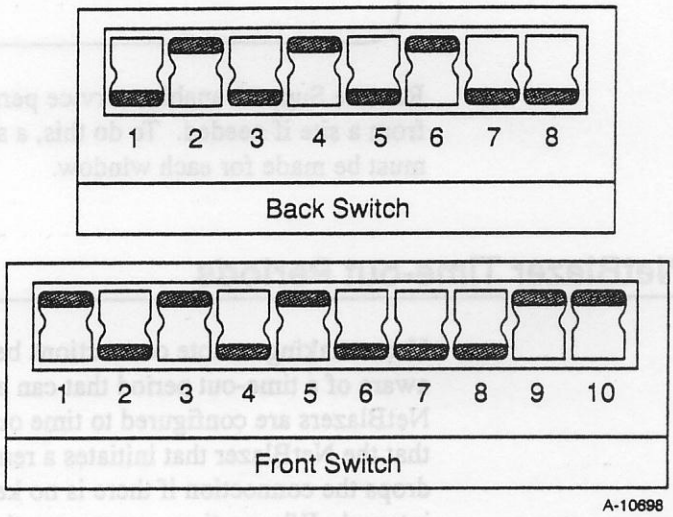


Figure 8-13. Switch Settings, Step 9

10. Once more, press the Reset button on the back of the modem and wait for the TST lamp on the front of the modem to go out.

11. Replace the front panel cover.

Establishing Remote Connections

Remote Support 3.0 provides an extended remote TCP/IP network connection to a site. Service personnel must first log in to a Communication Hub gateway before logging into a site. Log in by using the `telnet` command as described in the following subsection. Once a remote connection is made to the site maintenance workstation, diagnostic tests and other programs can be run on the Cray Research computer system and displayed on the remote host.

The `telnet` command is used to remotely log in to a remote system or host machine. The user must have a `login` on the machine they want to `telnet` to as shown in the following screen.

```
LocalHost: telnet host_name
Trying 147.219.x.x ...
Connected to host_name.
Escape character is '^]'.

login: user_name
Password:
```

Remote Support enables service personnel to open multiple windows from a site if needed. To do this, a separate `telnet` session to the site must be made for each window.

Telebit NetBlazer Time-out Periods

Users making remote connections between sites and services should be aware of a time-out period that can affect remote sessions. The Telebit NetBlazers are configured to time out after three minutes. This means that the NetBlazer that initiates a remote modem-to-modem connection drops the connection if there is no keyboard activity for any three-minute interval. When a time-out occurs, the `telnet` or `ftp` session continues to run. The NetBlazer automatically reestablishes the remote connection when the keyboard is used.

Transferring Files

The file transfer program (`ftp`) can be used to transfer files to and from a remote host machine. However, since connections between site and Service Center must go through a Communication Hub, file transfers must be transferred to the Hub before being transferred again to the destination host (an example of this process is described in the following "File Transfers Through a Communication Hub Gateway" subsection).

The client host with which `ftp` is to communicate may be specified on the command line. If this is done, `ftp` immediately attempts to establish a connection to an FTP server on that host; otherwise, `ftp` enters its command interpreter and waits for the user to enter commands. When `ftp` is waiting for commands from the user, it displays the `ftp>` prompt.

The `ftp` commands used most often are listed below.

`ascii`

Set the transfer format to ASCII (the default format). This command may be used to reset to ASCII transfers after transferring files in binary format.

`bell`
Sound a bell after each file transfer command is completed.

`binary`
Set the transfer format to binary. This command is used when transferring binary executable files.

`cd` *`remote_directory`*
Change the working directory on the remote machine to remote_directory.

`close`
Terminate the FTP session with the remote host and return to the `ftp>` prompt (command interpreter).

`dir [`*`remote_directory`*`]`
Print a list of files and subdirectories in the *`remote_directory`*. If no directory is specified, the current working directory on the remote machine is listed.

`get` *`remote_file`* `[`*`local_file`*`]`
Retrieve the `remote_file` and store it on the local machine. If a `local_file` is not specified, the transferred file is given the same name it has on the remote host.

`help [`*`command`*`]`
Print a single-line message about the meaning of a command. If no argument is given, `ftp` prints a list of all commands.

`ls [`*`remote_directory`*`] [`*`local_file`*`]`
Print an abbreviated listing of the contents of a directory on the remote host. If `remote_directory` is not specified, the current working directory is listed. If a `local_file` is not specified, the output is sent to the terminal.

`open` *`host_name`*
Establish a connection to the specified host FTP server from the `ftp>` prompt.

`put local_file [remote_file]`
Transfer the `local_file` to the remote host. If `remote_file` is not specified, the transferred file is named the same as the `local_file` name.

`pwd`
Print the name of the current working directory on the remote host.

`quit`
Quit or exit the `ftp` session.

`status`
Show the current status of the `ftp` session.

Aborting an ftp File Transfer

To abort an `ftp` file transfer, use the terminal interrupt key, which normally is **CTRL-C**.

Transferring Files Through a Communication Hub Gateway

File transfers between Service Centers and sites must go through a Communication Hub gateway. That is, the file is transferred to the Communication Hub gateway and transferred again to the destination host. Direct `ftp` file transfers between Service Centers and sites are not allowed.

NOTE: The following sample procedure describes how to transfer a file from a site through a Communication Hub gateway to a Service Center. The procedure begins at a Service Center location.

1. Use the `telnet` command to log in to the Communication Hub gateway as shown in the following screen.

```
LocalHost: telnet Hub_name
Trying 147.219.x.x ...
Connected to Hub_gate.
Escape character is '^]'.

login: user_name
Password:

Hub$
```

2. Use the `ftp` command to establish an `ftp` session to the site host as shown in the following screen.

```
$ ftp site_host
Connected to site_name.
220 Hub FTP server (SunOS 4.1) ready.
Name (host:UID): user_name
331 Password required for user_name.
Password:
230 User user_name logged in.
ftp>
```

3. Use any of the ftp commands listed earlier in this section to change directories and list the file that you want to transfer. In the following command the file *file_name* is located in the user's home directory and is listed with the **ls** command.

```
ftp> ls
200 PORT command successful.
150 Opening data connection for /bin/ls (ascii mode) (0 bytes)
.
.profile
field
file_name
mbox
tmp
226 Transfer complete.
510 bytes received in 0.093 seconds (5.4 Kbytes/s)
ftp>
```

4. Enter the following command to transfer a copy of the file (*file_name*) from the remote location (site) to the Communication Hub gateway. (The `put` command is used to transfer a file from a source host to the destination host.)

```
ftp> get file_name
200 PORT command successful.
150 Opening data connection for file_name (ascii mode) (57 bytes).
226 Transfer complete.
local: file_name remote: file_name
66 bytes received in 0.0046 seconds (14 Kbytes/s)
ftp>
```

5. Enter the following command to end the `ftp` session to the site host. The `ftp` process is still running on the Communication Hub gateway.

```
ftp> close
221 Goodbye.
ftp>
```

6. Establish an `ftp` session between the Hub and the Service Center host by entering the following commands.

```
ftp> open Service_Center-host
Connected to Service_Center-host
220 Site FTP server ($Header: ftpd.c 2.6 90/05/04 $) ready
.
Name (Service_Center-host:UID): user_name
331 Password required for user_name.
Password:
230 User user_name logged in.
ftp>
```

7. Enter the command shown in the screen below to transfer the file (*file_name*) from the Communication Hub gateway to the Service Center.

```
ftp> put file_name
200 PORT command successful.
150 ASCII data connection for ftp_test1 (137.38.61.2,1080).
226 ASCII Transfer complete.
ftp>
```

8. Enter the following command to end the `ftp` session between the gateway and Service Center and stop the `ftp` process that is running on the Communication Hub gateway.

```
ftp> quit
221 Goodbye.
Hub$
```

9. Log off the Communication Hub gateway to end the telnet session.

```
Hub$ exit
```

APPENDIX: CRAY Y-MP EL INSTRUCTION SET

	Instruction	CAL		Unit	Description
	000000	ERR			Error Exit
‡	0010*jk*	CA, A*j*	A*k*		Set the channel (Aj) CA register to (Ak) and begin I/O sequence
	001000	PASS			Pass
‡	0011*jk*	CL, A*j*	A*k*		Set the channel (Aj) CL register to (Ak)
‡	0012*j*0	C*i*, A*j*			Clear channel (Aj) interrupt and error flags; clear device Master Clear (output channel)
‡	0012*j*1	MC, A*j*			Clear channel (Aj) interrupt and error flags; set device Master Clear (output channel); clear device ready-held (input channel)
‡	0013*j*0	XA	A*j*		Transmit (Aj) to XA register
‡	0014*j*0	RT	S*j*		Transmit (Sj) to RTC register
‡	0014*j*1	SIPI	A*j*		Set Interprocessor Interrupt request to CPU (Aj)
	001401	SIPI			Set Interprocessor Interrupt of CPU 0
‡	001402	CIPI			Clear Interprocessor Interrupt
‡	0014*j*3	CLN	A*j*		Transmit (Aj) to CLN register
‡	0014*j*4	PCI	S*j*		Enter interrupt interval (II) register with (Sj)
‡	001405	CCI			Clear programmable clock interrupt (PCI) request
‡	001406	ECI			Enable PCI request
‡	001407	DCI			Disable PCI request
	001501				Disable all error correction
	001541				Enable replacement of check bytes with data on all ports writes to reads
	00200k	VL	A*k*		Transmit (Ak) to VL register
†	002000	VL	1		Transmit 1 to VL register
	002100	EFI			Enable interrupt on floating-point error
	002200	DFI			Disable interrupt on floating-point error
	002300	ERI			Enable operand range error interrupts
	002400	DRI			Disable operand range error interrupts
	002500	DBM			Disable bidirectional memory transfers
E	002504	DCBW			Disable concurrent block write

	Instruction	CAL		Unit	Description
E	002506	DSBO			Disable scalar and block overlap
	002600	EBM			Enable bidirectional memory transfers
E	002604	ECBW			Enable concurrent block write
E	002606	ESBO			Enable scalar and block overlap
	002700	CMR			Complete memory reference
	0030*j*0	VM	S*j*		Transmit (Sj) to VM register
†	003000	VM	0		Clear VM register
	0034*jk*	SM*jk*	1, TS		Test and Set semaphore *jk*; $0 \le jk \le 37_8$
	0036*jk*	SM*jk*	0		Clear semaphore *jk*; $0 \le jk \le 37_8$
	0037*jk*	SM*jk*	1		Set semaphore *jk*; $0 \le jk \le 37_8$
	004000	EX			Normal exit
	0050*jk*	J	B*jk*		Jump to (Bjk)
	006*ijkm*	*j*	*exp*		Jump to *exp* = *ijkm*
	007*ijkm*	R	*exp*		Return jump to *exp* = *ijkm*; set B00 to (P) + 2
	010*ijkm*	JAZ	*exp*		Jump to *exp* = *ijkm* if (A0) = 0 (2^2 of i = 0)
	011*ijkm*	JAN	*exp*		Jump to *exp* = *ijkm* if (A0) ≠ 0 (2^2 of i = 0)
	012*ijkm*	JAP	*exp*		Jump to *exp* = *ijkm* if (A0) positive (2^2 of i = 0)
	013*ijkm*	JAM	*exp*		Jump to *exp* = *ijkm* if (A0) negative (2^2 of i = 0)
	014*ijkm*	JSZ	*exp*		Jump to *exp* = *ijkm* if (S0) = 0 (2^2 of i = 0)
	015*ijkm*	JSN	*exp*		Jump to *exp* = *ijkm* if (S0) ≠ 0 (2^2 of i = 0)
	016*ijkm*	JSP	*exp*		Jump to *exp* = *ijkm* if (S0) positive (2^2 of i = 0)
	017*ijkm*	JSM	*exp*		Jump to *exp* = *ijkm* if (S0) negative (2^2 of i = 0)
	01*hijkm*	Ah	*exp*		Transmit *exp* = *ijkm* to A*h* (2^2 of i = 1)
‡†, X	020*iijkm*	A*i*	*exp*		Transmit *exp* = *jkm* to A*i*
‡†, Y	020*i*00*mn*	A*i*	*exp*		Transmit *exp* = *nm* to A*i*
‡†	021*ijkm*	A*i*	*exp*		Transmit one's complement of *exp* = *jkm* to A*i*
‡†, Y	021i00*mn*	A*i*	*exp*		Transmit one's complement of *exp* = *nm* to A*i*
‡†	022*ijk*	A*i*	*exp*		Transmit *exp* = *jk* to A*i*
	023*ij*0	A*i*	S*j*		Transmit (Sj) to A*i*
	023*i*01	A*i*	VL		Transmit (VL) to A*i*
	024*ijk*	A*i*	B*jk*		Transmit (Bjk) to A*i*

	Instruction	CAL		Unit	Description
	025*ijk*	B*jk*	A*i*		Transmit (Ai) to B*jk*
	026*ij*0	A*i*	PS*j*	S Pop	Transmit population count of (Sj) to A*i*
	026*ij*1	A*i*	QS*j*	S Pop	Transmit population count parity of (Sj) to A*i*
	026*ij*7	A*i*	SB*j*		Transmit (SBj) to A*i*
	027*ij*0	A*i*	ZS*j*	S/LZ	Transmit leading zero count of (Sj) to A*i*
	027*ij*7	SB*j*	A*i*		Transmit (Ai) to SB*j*
	030*ijk*	A*i*	A*j* + A*k*	A Int Add	Integer sum of (Aj) and (Ak) to A*i*
†	030*i*0*k*	A*i*	A*k*	A Int Add	Transmit (Ak) to A*i*
†	030*ij*0	A*i*	A*j* + 1	A Int Add	Transmit integer sum of (Aj) plus 1 to A*i*
	031*ijk*	A*i*	A*j* – A*k*	A Int Add	Integer difference of (Aj) less (Ak) to A*i*
†	031*i*00	A*i*	–1	A Int Add	Transmit –1 to A*i* (Ai = 37777777777) in Y-mode
†	031*i*0k	A*i*	–A*k*	A Int Add	Transmit the negative of (Ak) to A*i*
†	031*ij*0	A*i*	A*j* –1	A Int Add	Integer difference of (Aj) less 1 to A*i*
	032*ijk*	A*i*	A*j**A*k*	A Int Mult	Integer product of (Aj) and (Ak) to A*i*
	033*i*00	A*i*	CI		Transmit lowest interrupting channel number to A*i* (j = 0)
	033*ij*0	A*i*	CA, A*j*		Transmit address of channel (Aj) to A*i* (*j* ≠ 0)
	033*ij*1	A*i*	CE, A*j*		Transmit error flag of channel (Aj) to A*i* (*j* ≠ 0)
†	034*ijk*	B*jk*, A*i*	,A0	Memory	Read (Ai) words to B registers starting at B*jk* from memory address ((A0) + (DBA))
	034*ijk*	B*jk*, A*i*,	0, A0	Memory	Read (Ai) words to B registers starting at B*jk* from memory address ((A0) + (DBA))
	035*ijk*	,A0	B*jk*, A*i*	Memory	Write (Ai) words from B registers B*jk* to memory address ((A0) + (DBA))
†	035*ijk*	0, A0	B*jk*, A*i*	Memory	Write (Ai) words from B registers B*jk* to memory address ((A0) + (DBA))
	036*ijk*	T*jk*, A*i*	,A0	Memory	Read (Ai) words to T registers starting at T*jk* from memory address ((A0) + (DBA))
†	036*ijk*	T*jk*, A*i*	0, A0	Memory	Read (Ai) words to T registers starting at T*jk* from memory address ((A0) + (DBA))
	037*ijk*	,A0	T*jk*, A*i*	Memory	Write (Ai) words from T registers T*jk* to memory address ((A0) + (DBA))
†	037*ijk*	0, A0	T*jk*, A1	Memory	Write (Ai) words from T registers T*jk* to memory address ((A0) + (DBA))
X	040*ijkm*	S*i*	*exp*		Transmit *exp* = *jkm* to S*i*
Y	040*i*00*mn*	S*i*	*exp*		Transmit *exp* = *nm* to S*i*

	Instruction	CAL		Unit	Description
X	041*ijkm*	S*i*	*exp*		Transmit one's complement of *exp* = *jkm* to S*i*
Y	041*i*00*mn*	S*i*	*exp*		Transmit one's complement of *exp* = *nm* to S*i*
	042*ijk*	S*i*	<*exp*	S Logical	Form one's mask *exp* = 100_8 – *jk* bits in S*i* from the right
†	042*ijk*	S*i*	#>*exp*	S Logical	Form zeroes mask *exp* = *jk* bits in S*i* from the left
†	042*i*77	S*i*	1	S Logical	Enter 1 into S*i*
†	042*i*00	S*i*	–1	S Logical	Enter –1 into S*i* (Si = 177777 177777 177777 177777)
	043*ijk*	S*i*	>*exp*	S Logical	Form one's mask *exp* = *jk* bits in S*i* from the left
†	043*ijk*	S*i*	#<*exp*	S Logical	Form zeroes mask *exp* = 100_8 bits in S*i* from the right
†	043*i*00	S*i*	0	S Logical	Clear S*i*
	044*ijk*	S*i*	S*j*&S*k*	S Logical	Logical product of (Sj) and (Sk) to S*i*
†	044*ij*0	S*i*	S*j*&SB	S Logical	Sign bit of (Sj) to S*i*
†	044*ij*0	S*i*	SB&S*j*	S Logical	Sign bit of (Sj) to S*i* (j ≠ 0)
	045*ijk*	S*i*	#S*k*&S*j*	S Logical	Logical product of (Sj) and one's complement of (Sk) to S*i*
†	045*ij*0	S*i*	#SB&S*j*	S Logical	Transmit (Sj) with sign bit cleared to S*i*
	046*ijk*	S*i*	S*j*\S*k*	S Logical	Logical difference of (Sj) and (Sk) to S*i*
†	046*ij*0	S*i*	S*j*\SB	S Logical	Toggle sign bit of (Sj), enter into S*i*
†	046*ij*0	S*i*	SB\S*j*	S Logical	Toggle sign bit of (Sj), enter into S*i* (j ≠ 0)
	047*ijk*	S*i*	#S*j*\S*k*	S Logical	Logical equivalence of (Sk) and (Sj) to S*i*
†	047*i*0*k*	S*i*	#S*k*	S Logical	Transmit one's complement of (Sk) to S*i*
†	047*ij*0	S*i*	#S*j*\SB	S Logical	Logical equivalence of (Sj) and sign bit to S*i*
†	047*ij*0	S*i*	#SB\S*j*	S Logical	Logical equivalence of (Sj) and sign bit to S*i* (j ≠ 0)
†	047*i*00	S*i*	#SB	S Logical	Transmit one's complement of sign bit into S*i*
	050*ijk*	S*i*	S*j*\S*i*&S*k*	S Logical	Logical product of ((Si) and (Sk) complement) ORed with logical product of ((Sj) and (Sk)) to S*i* *scalar merge
†	050*ij*0	S*i*	S*j*\S*i*&SB	S Logical	Scalar merge of (Si) and sign bit of (Sj) to S*i*
	051*ijk*	S*i*	S*j*\S*k*	S Logical	Logical sum of (Sj) and (Sk) to S*i*
†	051*i*0*k*	S*i*	S*k*	S Logical	Transmit (Sk) to S*i*
†	051*ij*0	S*i*	S*j*\SB	S Logical	Logical sum of (Sj) and sign bit to S*i*

	Instruction	CAL		Unit	Description
†	051*ij*0	S*i*	SB!S*j*	S Logical	Logical sum of (Sj) and sign bit to S*i* (j ≠ 0)
†	051*i*00	S*i*	SB	S Logical	Transmit sign bit into S*i*
	052*ijk*	S0	S*i* < *exp*	S Shift	Shift (Si) left *exp* = *jk* places to S0
	053*ijk*	S0	S*i* > *exp*	S Shift	Shift (Si) right *exp* = 100_8 – *jk* places to S0
	054*ijk*	S*i*	S*i* < *exp*	S Shift	Shift (Si) left *exp* = *jk* places to S*i*
	055*ijk*	S*i*	S*i* > *exp*	S Shift	Shift (Si) right *exp* = 100_8 – *jk* places to S*i*
	056*ijk*	S*i*	S*i*, S*j* < A*k*	S Shift	Shift (Si and Sj) left (Ak) places to S*i*
†	056*ij*0	S*i*	S*i*, S*j* < 1	S Shift	Shift (Si and Sj) left one place to S*i*
†	056*i*0*k*	S*i*	S*i* < A*k*	S Shift	Shift (Si) left (Ak) places to S*i*
	057*ijk*	S*i*	S*j*, S*i* > A*k*	S Shift	Shift (Sj and Si) right (Ak) places to S*i*
†	057*ij*0	S*i*	S*j*, S*i* > 1	S Shift	Shift (Sj and Si) right one place to S*i*
†	057*i*0*k*	S*i*	S*i* > A*k*	S Shift	Shift (Si) right (Ak) places to S*i*
	060*ijk*	S*i*	S*j* + S*k*	S Int Add	Integer sum of (Sj) and (Sk) to S*i*
†	060*i*0*k*	S*i*	S*k*	S Int Add	Transmit (Sk) to S*i*
†	060*ij*0	S*i*	S*j* + S0	S int Add	Integer sum 2^{63} and (Sj) to S*i*
	061*ijk*	S*i*	S*j* – S*k*	S Int Add	Integer difference of (Sj) less (Sk) to S*i*
†	061*i*0*k*	S*i*	–S*k*	S Int Add	Transmit negative of (Sk) to S*i*
†	061*ij*0	S*i*	S*j* – S0	S Int Add	Integer difference of (Sj) less 2^{63} to S*i*
	062*ijk*	S*i*	S*j* – FS*k*	Fp Add	Floating-point sum of (Sj) and (Sk) to S*i*
†	062*i*0*k*	S*i*	+FS*k*	Fp Add	Normalize (Sk) to S*i*
	063*ijk*	S*i*	S*j* – FS*k*	Fp Add	Floating-point difference of (Sj) and (Sk) to S*i*
†	063*i*0*k*	S*i*	–FS*k*	Fp Add	Transmit normalized negative of (Sk) to S*i*
	064*ijk*	S*i*	S*j* * FS*k*	Fp Mult	Floating-point product of (Sj) and (Sk) to S*i*
	065*ijk*	S*i*	S*j* * HS*k*	Fp Mult	Half-precision rounded floating-point product of (Sj) and (Sk) to S*i*
	066*ijk*	S*i*	S*j* * RS*k*	Fp Mult	Full-precision rounded floating-point product of (Sj) and (Sk) to S*i*
	067*ijk*	S*i*	S*j* * IS*k*	Fp Mult	Two minus the floating-point product of (Sj) and (Sk) to S*i*
	070*ij*0	S*i*	/HS*j*	Fp Recp	Floating-point reciprocal approximation of (Sj) to S*i*
	071*i*0*k*	S*i*	A*k*		Transmit (Ak) to S*i* with no sign extension
	071*i*1*k*	S*i*	+A*k*		Transmit (Ak) to S*i* with sign extension
	071*i*2*k*	S*i*	+FA*k*		Transmit (Ak) to S*i* as unnormalized floating-point number (exponent = 40060)

	Instruction	CAL		Unit	Description
	071*i*30	S*i*	0.6		Transmit constant 0.75 x 2^{48} to S*i* (Si = 040060 140000 000000 000000)
	071*i*40	S*i*	0.4		Transmit constant 0.5 to S*i* (Si = 040000 100000 000000 000000)
	071*i*50	S*i*	1.0		Transmit constant 1.0 to S*i* (Si = 040001 100000 000000 000000)
	071*i*60	S*i*	2.0		Transmit constant 2.0 to S*i* (Si = 040002 100000 000000 000000)
	071*i*70	S*i*	4.0		Transmit constant 4.0 to S*i* (Si = 040003 100000 000000 000000)
	072*i*00	S*i*	RT		Transmit (RTC) to S*i*
	072*i*02	S*i*	SM		Transmit (SM) to S*i*
	072*ij*3	S*i*	ST*j*		Transmit (STj) to S*i*
	073*i*00	S*i*	VM		Transmit (VM) to S*i*
	073*i*01	S*i*	SR*j*		Transmit status register (SRj) bits to S*i*
	073*i*11	¶¶			Read performance counter to S*i*
E	073*i*31	¶¶			Clear memory maintenance modes and read status register into S*i*
	073*i*02	SM	S*i*		Transmit (Si) to SM
	0731*j*3	ST*j*	S*i*		Transmit (Si) to ST*j*
	074*ijk*	S*i*	T*jk*		Transmit (Tjk) to S*i*
	075*ijk*	T*jk*	S*i*		Transmit (Si) to T*jk*
	076*ijk*	S*i*			Transmit (V*j*, element (Ak)) to S*i*
	077*ijk*	V*i*, A*k*	S*j*		Transmit (Sj) to V*i* element (Ak)
†	077*i*0*k*	V*i*, A*k*	0		Clear V*i* element (Ak)
X	10*hijkm*	A*i*	*exp*, A*h*	Memory	Read from memory address ((Ah) + jkm + (DBA)) to A*i* (h ≠ 0)
Y	10*hi*00*mn*	A*i*	*exp*, A*h*	Memory	Read from memory address ((Ah) + nm + (DBA)) to A*i* (h ≠ 0)
†, X	100*ijkm*	A*i*	*exp*, 0	Memory	Read from memory address (jkm + (DBA)) to A*i*
Y	100*i*00*mn*	A*i*	*exp*, 0	Memory	Read from memory address (nm + (DBA)) to A*i*
†, X	100*ijkm*	A*i*	*exp*,	Memory	Read from memory address (jkm + (DBA)) to A*i*
Y	100*i*00*mn*	A*i*	*exp*,	Memory	Read from memory address (nm + (DBA)) to A*i*
X	10*hi*000	A*i*	,A*h*	Memory	Read from memory address ((Ah) + (DBA)) to A*i* (h ≠ 0)
Y	10*hi*0000	A*i*	,A*h*	Memory	Read from memory address ((Ah + (DBA)) to A*i* (h ≠ 0)
X	11*hijkm*	*exp*,A*h*	A*i*	Memory	Write (Ai) to memory address ((Ah) + jkm + (DBA)) (h ≠ 0)

	Instruction	CAL		Unit	Description
Y	11*hi*00*mn*	*exp*,A*h*	A*i*	Memory	Write (Ai) to memory address ((Ah) + nm + (DBA)) (Ah ≠ 0)
†, X	110*ijkm*	*exp*,0	A*i*	Memory	Write (Ai) to memory address (jkm + (DBA))
Y	110*i*00*mn*	*exp*,0	A*i*	Memory	Write (Ai) to memory address (nm + (DBA))
†, X	110*ijkm*	*exp*,	A*i*	Memory	Write (Ai) to memory address (jkm + (DBA))
Y	110*i*00*mn*	*exp*,	A*i*	Memory	Write (Ai) to memory address (nm + (DBA))
†, X	11*hi*000	,A*h*	A*i*	Memory	Write (Ai) to memory address ((Ah) + (DBA)) (h ≠ 0)
Y	11*hi*0000	,A*h*	A*i*	Memory	Write (Ai) to memory address ((Ah + (DBA)) (h ≠ 0)
X	12*hijkm*	S*i*	*exp*,A*h*	Memory	Read from memory address ((Ah) + jkm + (DBA)) to S*i* (h ≠ 0)
Y	12*hi*00*mn*	S*i*	*exp*,A*h*	Memory	Read from memory address ((Ah) + nm + (DBA)) to S*i* (h ≠ 0)
X	120*ijkm*	S*i*	*exp*,0	Memory	Read from memory address (jkm + (DBA)) to S*i*
Y	120*i*00*mn*	S*i*	*exp*,0	Memory	Read from memory address (nm + (DBA)) to S*i*
X	120*ijkm*	S*i*	*exp*,	Memory	Read from memory address (jkm + (DBA)) to S*i*
Y	120*i*00*mn*	S*i*	*exp*,	Memory	Read from memory address (nm + (DBA)) to S*i*
, X	12*hi*000	S*i*	,A*h*	Memory	Read from memory address ((Ah) + (DBA)) to S*i* (h ≠ 0)
Y	12*hi*0000	S*i*	,A*h*	Memory	Read from memory address ((Ah) + (DBA)) to S*i* (h ≠ 0)
X	13*hijkm*	*exp*,A*h*	S*i*	Memory	Write (Si) to memory address ((Ah) + jkm + (DBA)) (h ≠ 0)
Y	13*hi*00*mn*	*exp*,A*h*	S*i*	Memory	Write (Si) to memory address ((Ah) + nm + (DBA)) (h ≠ 0)
†, X	130*ijkm*	*exp*,0	S*i*	Memory	Write (Si) to memory address (jkm + (DBA))
Y	130*i*00*mn*	*exp*,0	S*i*	Memory	Write (Si) to memory address (nm + (DBA))
X	130*ijkm*	*exp*,	S*i*	Memory	Write (Si) to memory address (jkm + (DBA))
Y	130*i*00*mn*	*exp*,	S*i*	Memory	Write (Si) to memory address (nm + (DBA))
X	13*hi*000	,A*h*	S*i*	Memory	Write (Si) to memory address ((Ah) + (DBA)) (h ≠ 0)
Y	13*hi*0000	,A*h*	S*i*	Memory	Write (Si) to memory address ((Ah) + (DBA)) (h ≠ 0)

	Instruction	CAL		Unit	Description
	140*ijk*	V*i*	S*j*&V*k*	V Logical	Logical products of (Sj) and (Vk) to V*i*
	141*ijk*	V*i*	V*j*&V*k*	V Logical	Logical products of (Vj) and (Vk) to V*i*
	142*ijk*	V*i*	Sj!V*k*	V Logical	Logical sums of (Sj) and (Vk) to V*i*
†	142*i*0*k*	V*i*	V*k*	V Logical	Transmit (Vk) to V*i*
	143*ijk*	V*i*	V*j*!V*k*	V Logical	Logical sums of (Vj) and (Vk) to V*i*
	144*ijk*	V*i*	S*j*\V*k*	V Logical	Logical differences of (Sj) and (Vk) to V*i*
	145*ijk*	V*i*	V*j*\V*k*	V Logical	Logical differences of (Vj) and (Vk) to V*i*
†	145*iii*	V*i*	0	V Logical	Clear V*i*
	146*ijk*	V*i*	S*j*! V*k*&VM	V Logical	Transmit (Sj) if VM bit = 1; (Vk) if VM bit = 0 to V*i* *scalar *vector merge
†	146*i*0*k*	V*i*	#VM&V*k*	V Logical	Vector merge of (Vk) and 0 to V*i*
	147*ijk*	V*i*	V*j*! V*k*&VM	V Logical	Transmit (V*j*) if VM bit = 1; (Vk) if VM bit = 0 to V*i* *vector *vector merge
	150*ijk*	V*i*	V*j* < A*k*	V Shift	Shift (Vj) left (Ak) places to V*i*
	150*ij*0	V*i*	V*j* < 1	V Shift	Shift (Vj) left one place to V*i*
	151*ijk*	V*i*	V*j* > A*k*	V Shift	Shift (Vj) right (Ak) places to V*i*
	151*ij*0	V*i*	V*j* > 1	V Shift	Shift (Vj) right one place to V*i*
	152*ijk*	V*i*	V*j*,V*j* < A*k*	V Shift	Double shift (Vj) left (Ak) places to V*i*
†	152*ij*0	V*i*	V*j*,V*j* < 1	V Shift	Double shift (Vj) left one place to V*i*
	153*ijk*	V*i*	V*j*,V*j* > A*k*	V Shift	Double shift (Vj) right (Ak) places to V*i*
	153*ij*0	V*i*	V*j*,V*j* > 1	V Shift	Double shift (Vj) right one place to V*i*
	154*ijk*	V*i*	S*j* + V*k*	V Int Add	Integer sums of (Sj) and (Vk) to V*i*
	155*ijk*	V*i*	V*j* + V*k*	V Int Add	Integer sums of (Vj) and (Vk) to V*i*
	156*ijk*	V*i*	S*j* – V*k*	V Int Add	Integer differences of (Sj) and (Vk) to V*i*
	156*i*0*k*	V*i*	–V*k*	V Int Add	Transmit negative of (Vk) to V*i*
	157*ijk*	V*i*	V*j* – V*k*	V Int Add	Integer differences of (Vj) and (Vk) to V*i*
	160*ijk*	V*i*	S*j* * FV*k*	Fp Mult	Floating-point products of (Sj) and (Vk) to V*i*
	161*ijk*	V*i*	V*j* * FV*k*	Fp Mult	Floating-point products of (Vj) and (Vk) to V*i*
	162*ijk*	V*i*	S*j* * HV*k*	Fp Mult	Half-precision rounded floating-point products of (Sj) and (Vk) to V*i*
	163*ijk*	V*i*	V*j* * HV*k*	Fp Mult	Half-precision rounded floating-point products of (V*j*) and (Vk) to V*i*
	164*ijk*	V*i*	S*j* * RV*k*	Fp Mult	Rounded floating-point products of (Sj) and (Vk) to V*i*
	165*ijk*	V*i*	V*j* * RV*k*	Fp Mult	Rounded floating-point products of (V*j*) and (Vk) to V*i*
X	166*ijk*	V*i*	S*j* * IV*k*	Fp Mult	Two minus the floating-point products of (Sj) and (Vk) to V*i*
Y	166*ijk*	V*i*	S*j* * V*k*	Fp Mult	32-bit integer products of (Sj) and (Vk) to V*i*

	Instruction	CAL		Unit	Description
	167*ijk*	V*i*	V*j* * IV*k*	Fp Mult	Two minus the floating-point products of (Vj) and (Vk) to V*i*
	170*ijk*	V*i*	S*j* + FV*k*	Fp Add	Floating-point sums of (Sj) and (Vk) to V*i*
†	170*i*0*k*	V*i*	+FV*k*	Fp Add	Normalize (Vk) to V*i*
	171*ijk*	V*i*	V*j* + FV*k*	Fp Add	Floating-point sums of (Vj) and (Vk) to V*i*
	172*ijk*	V*i*	S*j* – FV*k*	Fp Add	Floating-point differences of (Sj) and (Vk) to V*i*
†	172*i*0*k*	V*i*	–FV*k*	Fp Add	Transmit normalized negatives of (Vk) to V*i*
	173*ijk*	V*i*	V*j* – FV*k*	Fp Add	Floating-point differences of (Vj) and (Vk) to V*i*
	174*ij*0	V*i*	/HV*j*	Fp Recp	Floating-point reciprocal approximations of (Vj) to V*i*
	174*ij*1	V*i*	PV*j*	V Pop	Population counts of (Vj) to V*i*
	174*ij*2	V*i*	QV*j*	V Pop	Population count parities of (Vj) to V*i*
	1750*j*0	VM	V*j*,Z	V Logical	VM = 1 if (Vj) = 0
	1750*j*1	VM	V*j*,N	V Logical	VM = 1 if (Vj) ≠ 0
	1750*j*2	VM	V*j*,P	V Logical	VM = 1 if (Vj) positive; 0 is positive
	1750*j*3	VM	V*j*,M	V Logical	VM = 1 if (Vj) negative; 1 is negative
	175*ij*4	V*i*,VM	V*j*,Z	V Logical	VM bit = 1 if (Vj element) = 0 and element index is loaded into (compressed Vi)
	175*ij*5	V*i*,VM	V*j*,N	V Logical	VM bit = 1 if (Vj element) ≠ 0 and element index is loaded into (compressed Vi)
	175*ij*6	V*i*,VM	V*j*,P	V Logical	VM bit = 1 if (Vj element) ≥ 0 and element index is loaded into (compressed Vi)
	175*ij*7	V*i*,VM	V*j*,M	V Logical	VM bit = 1 if (Vj element) < 0 and element index is loaded into (compressed Vi)
	176*i*0*k*	V*i*	A0,A*k*	Memory	Read (VL) words to V*i* from memory address ((A0) + (DBA)) incremented by (Ak)
	176*i*00	V*i*	A0,1	Memory	Read (VL) words to V*i* from memory address ((A0 + (DBA)) incremented by 1
	176*i*1*k*	V*i*	A0,V*k*	Memory	Read (VL) words to V*i* from memory address ((A0 + (Vk) + (DBA)) *gather
	1770*jk*	,A0,A*k*	V*j*	Memory	Write (VL) words from V*j* to memory address ((A0) + (DBA)) incremented by (Ak)

Instruction	CAL		Unit	Description
1770*j*0	,A0, 1	V*j*	Memory	Write (VL) words from V*j* to memory address ((A0) + (DBA)) incremented by 1
1771*jk*	,A0,V*k*	V*j*	Memory	Write (VL) words from V*j* to memory address ((A0) + (Vk) + (DBA)) *scatter

† – Special syntax mode
‡ – Priviledged to monitor mode
‡† – Generated depending on *exp*.
¶¶ – Not supported by CAL version 2
X – X-mode instruction
Y – Y-mode instruction
E – E-mode instruction
( ) – Read as *the contents of* ...

Register	Value
Ah, h = 0	0
Ai, i = 0	(A0)
Aj, j = 0	0
Ak, k = 0	1
Si, i = 0	(S0)
Sj, j = 0	0
Sk, k = 0	2^{63}